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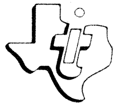
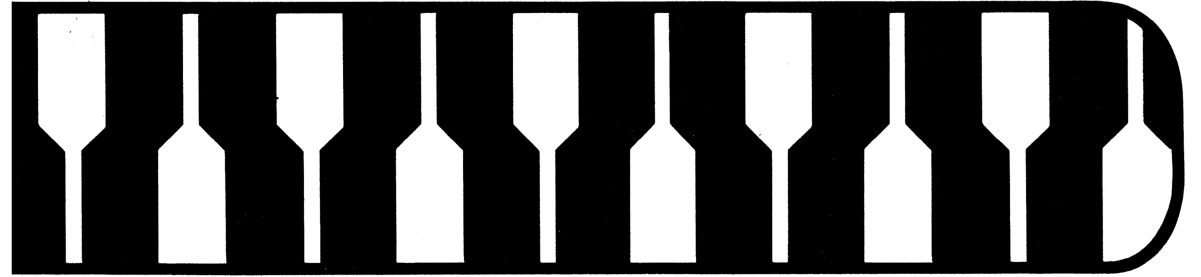


TMS4164 64K Dynamic RAM Reliability Report



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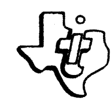

TMS4164 64K Dynamic RAM Reliability Report

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TMS 4164 RELIABILITY REPORT

ABSTRACT

This report describes the TMS 4164 Quality and Reliability program at Texas Instruments. Both component and system reliability levels of achievement are presented. Also included in this report are definitions of pertinent quality and reliability parameters to enable the reader to approach these subjects from the same frame of reference as the authors.

The program is a natural outgrowth of Texas Instruments philosophy of system design to achieve customer reliability goals. A long term TI commitment to producing quality components assures our customers that their system will exhibit superior reliability. An example of this continuous effort toward outstanding reliability is the story of the development of TMS 4164 presented here.

INTRODUCTION

BACKGROUND

The first MOS integrated circuits were produced at TI over 15 years ago. Since that time the N-channel silicon gate MOS process has experienced a long history of high-volume production resulting in a mature, stable, and reliable manufacturing process. This same N-MOS process was selected for the dynamic random-access memory (DRAM)* family of components because of this fine track record.

The system designer is interested in reliability for several reasons. He usually has requirements imposed on his system that can be met only if the individual components and cumulative design perform within specified limits for predetermined periods of time. These requirements all contribute to the problem that his final decision-making must solve for system reliability. To make the right choices he must know the reliability goals he is designing to and the parameters he must meet.

At this point it is wise to have a firm mental grasp of the impacts of component quality and reliability control. The following definitions should help in clarifying these important concepts.

DEFINITIONS

Quality. The quality of a product is the measure of the degree to which a combination of design and manufacturing expertise conforms to customer requirements at a time baseline we can term "time zero". Quality can be designated as the probability of defective units appearing in a given lot when initially received by the ultimate user. While zero defective items is the ideal goal, there will usually be some percentage of defective units in the lot. The quantity of these units is inversely related to not only quality of design and production that goes into the part but also rigor of the outgoing inspection the part receives.

Reliability. This term is defined as the probability that a unit will operate for a continuous period of time under a given set of operating conditions without failure. Failure is defined as a loss of capability in performing a required function. The time element is the principal difference between quality and reliability. Reliability is, in effect, a measure of how long quality lasts.

System Reliability. This, in the field, is a function of the total reliability of system components and the design implementing these components. Present large-scale integration techniques relieve today's system designers of many reliability concerns by providing "systems on a chip" with built-in reliability. Much of the system reliability concern is then shifted to the component design process. This subject will be discussed further on.

It is well known that the higher the level of device integration, the lower the failure rate on a per-function basis. The reduced interconnection requirement results in fewer wirebond and other such age-related failures. Many systems exhibit series reliability and, assuming a constant component failure rate, can be calculated by simply adding the individual component failure rates. System reliability considerations are covered in more detail in the Quality and Reliability Program section.

Component Reliability. Systems designers are concerned with the contribution of each component to the system failure rate. The component reliability is frequently expressed as a rate (percent per 1000 hours, FITs failures per 10^9 hours etc.) or a time such as MTBF (mean time between failures). The ultimate consideration, however, is its impact on the system. This may be a question of contribution to systems during warranty, system field repair intervals, etc. We will discuss later, in some detail, the significance of component reliability and the factors involved in current advanced LSI technologies.

Achieving high quality and long-term reliability in any product costs money, manpower, and time. The amount of money is related to the production rate, design reliability goals, and equipment necessary to measure progress in achieving the desired goals. The personnel involved must be dedicated to quality and interested in how their job functions impact on final test processes and device tests. Time is required both to develop a history of reliable processing and to produce the actual quality and reliability data that is needed to project future reliability goals.

* Dynamic random-access memories, (DRAMs) also known as read/write memories, are today's most widely used, efficient memory devices in large mainframe, minicomputer, and microcomputer systems. They have successfully replaced magnetic core memories as the medium for main memory storage since the early seventies.

BACKGROUND

Quality must begin before the first wafers are processed. Reliability is a result of a history of designing-in quality. The evolution of dynamic RAMs is a story of the MOS technology coupled with innovative circuit design techniques. On-chip address translation and decoding with TTL-compatible input/output circuitry make the present day N-channel, silicon gate, 5-volt-only 64K DRAM, such as the TMS 4164, easy to use in any kind of memory-intensive system.

CELL

The 6-transistor flip-flop of the late sixties was the basic cell used in static RAMs. Although there are a few variations of this cell, e.g., depletion loads, poly-resistor loads, etc., the static RAM cells of the early eighties maintain these characteristics. The DRAM cell gradually evolved from the 6-transistor cell (Figure 1) to the 3-transistor cell (Figure 2) and finally the 1-transistor cell (Figure 3). The 3-transistor cell was used in the P-channel silicon gate 1103 DRAM (1024 words × 1 bit), the first popularly accepted DRAM.

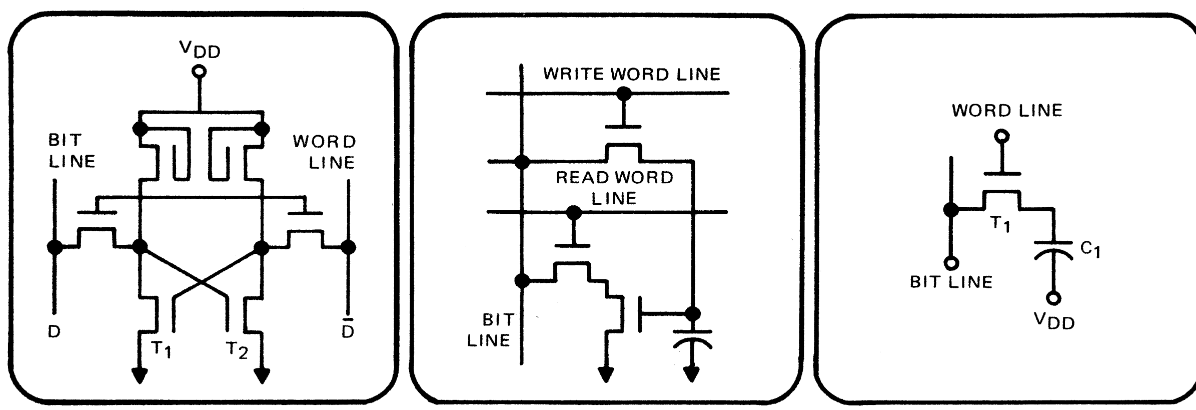


FIGURE 1 – 6-TRANSISTOR STATIC RAM CELL

FIGURE 2 – 3-TRANSISTOR DRAM CELL

FIGURE 3 – 1-TRANSISTOR DRAM CELL

As proven by the 4K DRAM (TMS 4030, TMS 4060, TMS 4027) and later the industry standard 16K DRAM (TMS 4116) and 64K DRAM (TMS 4164), the basic 1-transistor/1-capacitor cell has become the workhorse for data storage. The operation of this cell is described below.

Transistor T1 is designated the access transistor or transfer gate, and it acts as a 2-way switch to propagate data to or from the bit line to the storage capacitor, C1. C1 is a conventional MOS capacitor whose field plate is connected to a fixed positive potential V_{DD} (nominally 5 volts) as shown in Figure 4. This figure depicts a scaled double level poly-transistor cell. The poly-1 field plate connected to V_{DD} drops enough potential across the SiO_2 dielectric to form an inversion layer in the silicon underneath the electrode.

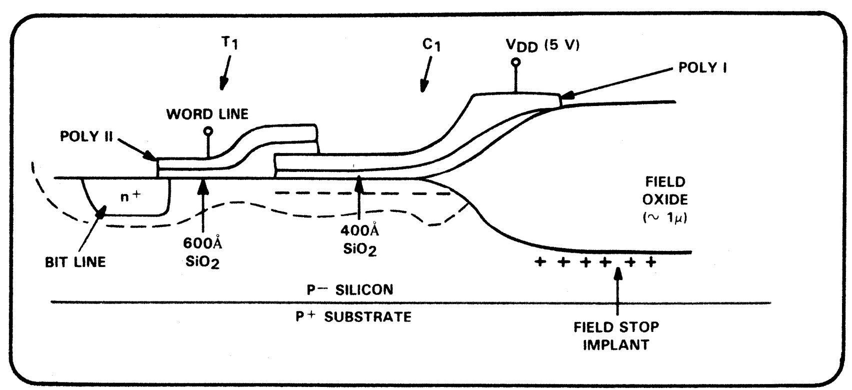


FIGURE 4 – SCALED DOUBLE LEVEL POLY-TRANSISTOR CELL

When a true logic "0" is to be stored, the n+ diffused bit line is brought to V_{SS} (0 volts), and the access transistor, T_1, is turned on (V_{DD}+). The storage node, which is at the Si-SiO_2 interface, is discharged to V_{SS}. When the word line is brought to V_{SS}, the storage node remains filled with electrons (minority carriers for an N-channel RAM). Conversely, if a logic "1" were to be stored, the bit line would be brought to V_{DD}, thus depleting all the electrons at the storage node. During store, the word line potential is not expected to ever exceed one threshold voltage above V_{SS} for unselected word lines. (Reliable operation of the RAM demands very quiet word lines. Active bleeder devices in TMS 4164 hold the unselected word lines at ground potential during the critical sensing amplification period.) Minimal sub-threshold leakage through the transfer gate is also assured in TMS 4164 by precharging the bit lines to V_{DD}, thus supplying the most positive voltage available on the source node of the access device. Use of epitaxial silicon for the top several microns of substrate ensures excellent refresh times under worst-case operating conditions.

SENSE AMPLIFIER

With added complexities and large densities, effective sensing circuitry has become mandatory for reliable memory operation. In TMS 4164 the 8-row addresses provide a 1-out-of-256 row selection and the 8-column addresses provide 1-out-of-256 column selection. The 64K dynamic RAM is optimally organized as a 256-row × 256-column matrix to operate the chip at minimal power dissipation (enhancing system reliability through relatively cooler chip temperature). The on-chip circuitry, including decoders, clocks, etc., is shown in Figure 5.

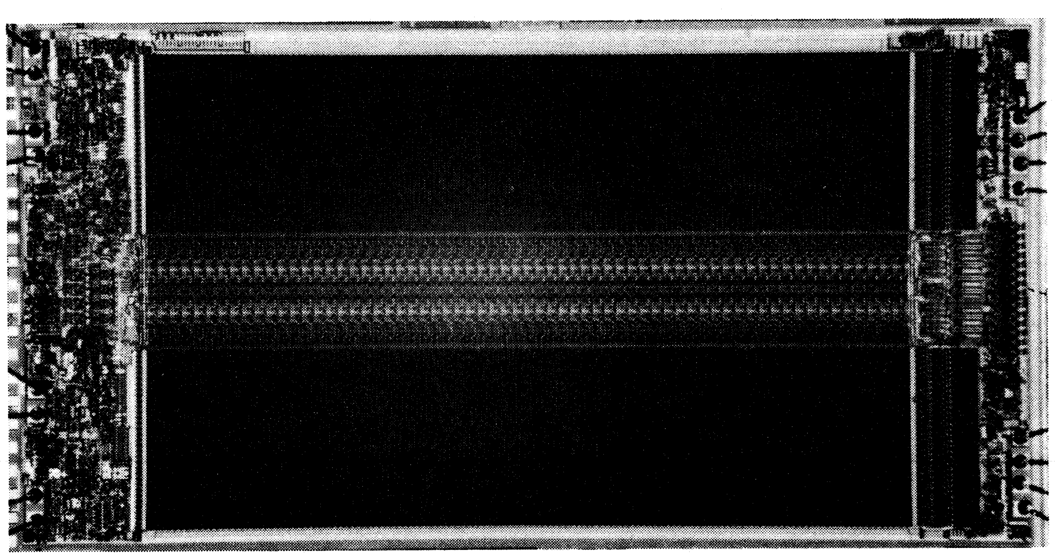


FIGURE 5 – TMS 4164 BAR PHOTOGRAPH

The basic detection circuitry is a dynamic differential amplifier. This amplifier is expected to detect a signal as small as 100 millivolts worst-case (C-storage/C-bit line is approximately 0.07 in TMS 4164) and amplify this signal by a factor of 50 in less than 30 nanoseconds. In addition the differential amplifier must dissipate less than 0.1 milliwatt in any given cycle (25.6 mW per device).

The sense amplifier, popular in the early seventies, is a static differential amplifier shown in Figure 6. The bit lines are precharged to $V_{SS} + V_T$ and are equalized through transistor, T3. The dummy storage capacitance, C_{dummy}, is about $C_S/2$. The word line for the selected bit and the dummy bit are on the opposite side of the differential amplifier between the two bit lines (whether "0" or "1" is read out of the bit). A small differential voltage is established on the bit lines when the storage all transfer gate, T_S, and the dummy cell transfer gate, T_{dummy}, are turned on. The loads T1 and T2 are activated, and the amplification process is completed through the flip-flop action as with a conventional static flip-flop.

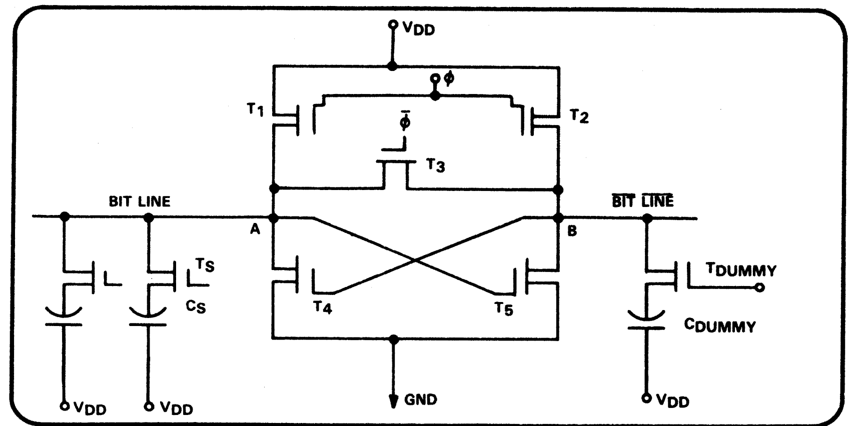


FIGURE 6 – EARLY SEVENTIES SENSE AMPLIFIER

The disadvantages of this amplifier are excessive power dissipation (amplifier has a dc path almost all the time when CE is high or $\overline{RAS}$ is low), direct loading of bit line capacitance on sensing nodes A and B and excessive bit line capacitance (precharge to V_{SS} only $C_{JN} \alpha (V_{JN})^{-1/2}$. These problems have been partly solved in early 16K DRAM designs. A typical sense amplifier used in l6K DRAMs is shown in Figure 7.

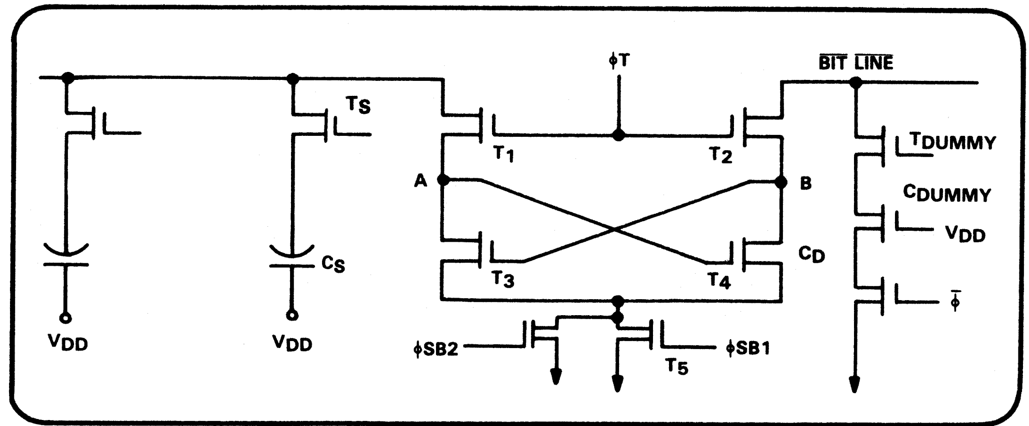


FIGURE 7 – TYPICAL SENSE AMPLIFIER FOR 16K DRAMS

The dynamic sense amplifier shown above isolates the large bit line capacitance from the sensing nodes A and B by means of isolation devices T1 and T2 thus speeding up sensing action. By modulating phase ϕ_T, T1 and T2 offer high impedance in pre-sense and low impedance in post-sense action. Bit line capacitance is reduced by precharging bit lines to V_{DD}. The activation of amplification circuitry is accomplished through a 2-step sequential activation of phase SB1 and phase SB2. Although this sense amplifier, when compared to the amplifier shown in Figure 6, conserved power and sped up the overall sensing process, it lacked an effective method of writing a full "1" level back into the storage node when "1" is read out or written in. This is accomplished in the sense amplifier used in TI's 64K DRAM (U.S. Patent 4, 239, 993). The key elements are shown in Figure 8.

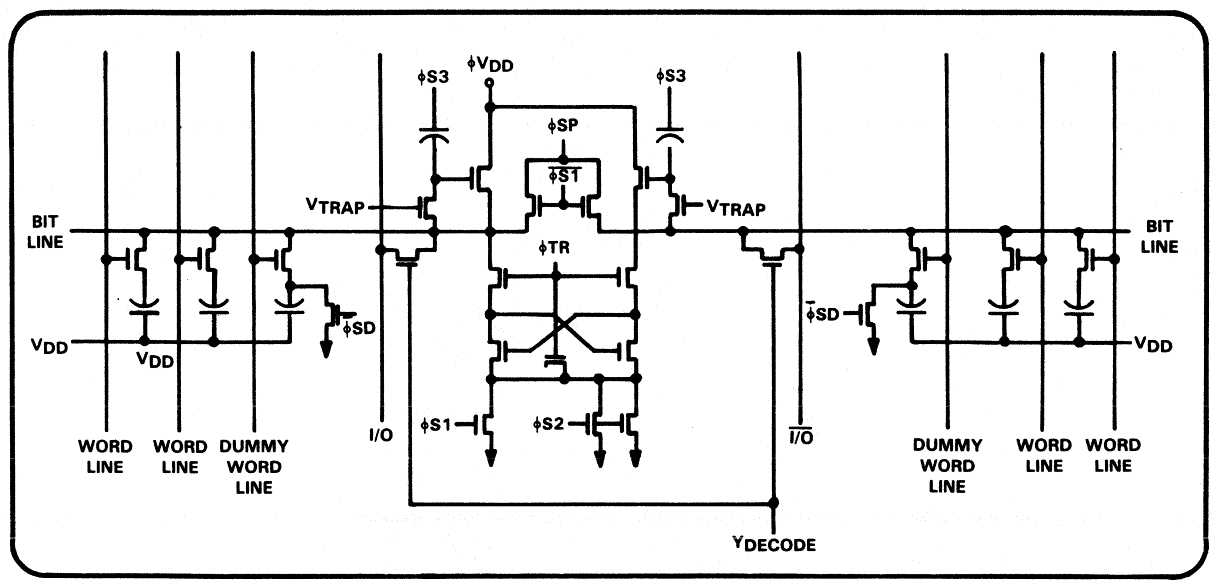


FIGURE 8 – TEXAS INSTRUMENTS 64K DRAM SENSE AMPLIFIER

Note that restoring full "1" level:

(1) Enhances refresh time and inherent design margins

(2) Gives capability for extended page operation

After sensing, dynamic loads are activated. This minimizes "bump" on active low-going bit lines, conserves average power, and lowers I_{DD} transient peaks. The selected word line is booted above V_{DD} while restoring the read datum.

PERIPHERAL CIRCUITRY

For better component reliability and avoidance of timing glitches internal to the chip, the on-chip clock design on TMS 4164 uses a novel interlock system. While the older-generation DRAM on-chip clock generators relied entirely on gate delays, and thus were susceptible to internal race conditions, TMS 4164 employs interlock clock schemes that render the working chip relatively immune to parametric variations in the manufacturing process. For example, until the word line decoding has been completed, the word line (to the access transistors) will not be activated. This technique also helps to reduce I_{DD} peaks to less than 70 milliamperes (typically).

The TMS 4164 is designed with separate on-chip address buffers for row and column address detection and subsequent voltage amplification (minimum TTL levels to full V_{DD}/V_{SS} internal to the chip). Use of separate address buffers eliminates the need for complex multiplexing and clocking circuitry, and also provides increased margins for address setup and hold times. An on-chip finely-tuned reference generator coupled with very sensitive 3-stage dynamic input differential amplifiers allow accurate, quick address level detection. Use of epitaxial silicon provides an excellent sink for minority carriers within a few microns (far less than 1 diffusion length). This enables the TMS 4164 to tolerate typically −1 volt dc levels, and up to −3 volt transients on inputs. Series poly resistors and N+/P− junctions at the bondpads (addresses) provide adequate filtering action and level capture.

MODELING DURING DESIGN

The design is not complete with the circuit description and electrical schematic. Using the desired propagation delays and circuit description, the logic is modeled for proper device operation using various computer simulations. When logic has been verified, the design is then adapted to simulation programs that calculate device performance based on the capacitance and resistances involved in the various process materials. These programs comprehend process variations which the designer must account for (V_T windows, poly widths, etc.) and then suggest the required layout of logic on the actual chip to maximize speed performances and minimize noise and power providing high quality and reliability. The simulation programs are linked to Computer Aided Design (CAD) stations (Figure 9) where actual layout of the device is generated. Each of the masks used in wafer fabrication is stored on tape and may be modified or updated at the CAD station.

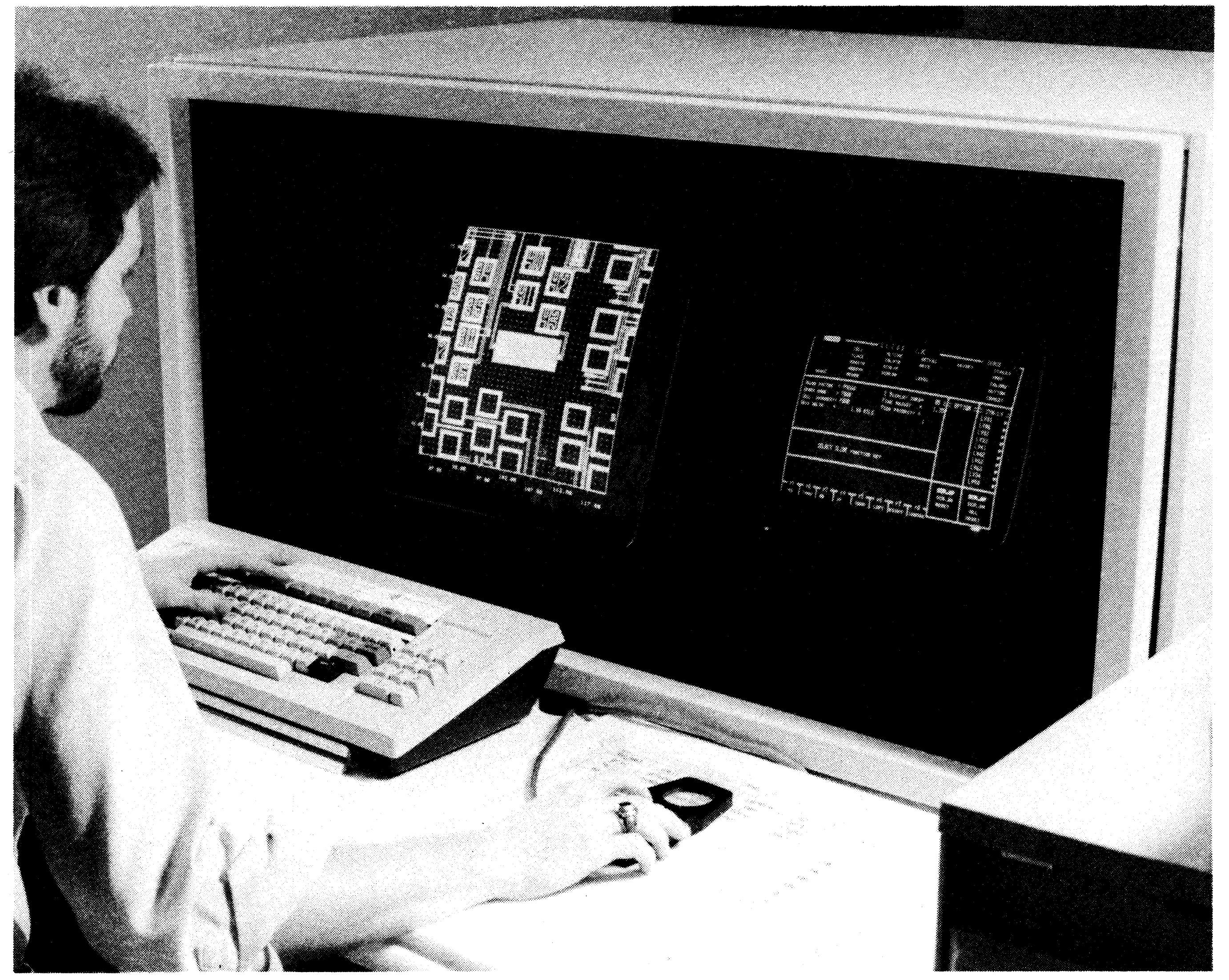


FIGURE 9 – COMPUTER AIDED DESIGN (CAD) TERMINAL

PROCESSING STEPS

A detailed description of the manufacture of the TMS 4164 is not practical in this report; however, the ultimate quality of the part is a direct result of the way in which it was fabricated. Consideration of some of the processing steps and their effects serves to demonstrate this relationship.

One of the unique features of the TMS 4164 is that it is fabricated on a lightly doped P− epitaxial silicon layer grown on a heavily doped P+ substrate. The heavily doped P+ substrate provides the following:

(1) Highly conductive ground plane that minimizes noise coupling into critical sensing circuitry from the input pads when inputs are allowed to swing from V_{IHMAX} to V_{ILMIN} (almost an 8-volt swing in less than 5 nanoseconds). Other sources of noise are similarly damped.

(2) Relatively inferior charge lifetime so as to be an excellent minority carrier sink

(3) Excellent backside contact in package minimizing sensitivity to complex data patterns

The lightly doped P− epitaxial layer provides:

(1) Relatively high minority carrier lifetime, guaranteeing excellent data storage time for the array (translates into long refresh times at elevated temperature)

(2) Relative freedom from heavy metallic contents, minimizing undesirable array/peripheral leakages (junction, field-induced)

The interface of the P−/P+ substrate furnishes a good minority carrier sink due to an interface with a large gradation of impurity concentration variation. (MOS, being a surface-oriented device, requires a very high quality 2 to 3 micron deep region underneath the field plates and junctions.) These attributes of TMS 4164 give it an excellent tolerance to data patterns and assure data integrity under worst-case voltage/temperature input conditions. Figure 10 shows a typical Shmoo plot highlighting extreme tolerances to input level swings beyond the data sheet specifications at 88°C. Table 1 demonstrates the advantages of epitaxial silicon in preserving long refresh times even at 90° case temperatures. The table gives typical refresh times for TMS 4164s constructed under the same process and design rules with the only difference being the EPI layer on one group. It can be seen from this data that a significant improvement in refresh times is shown in the EPI crystal.

Another advantage of the epitaxial layer is enhanced performance of the diffused guard rings. These rings are diffused around each array half and are biased to V_{DD} during operation. This creates a depletion region around the arrays making it nearly impossible for minority carriers to penetrate. Empirical data shows that this guard ring is at least five orders of magnitude more effective using the epitaxial layer versus a homogeneous crystal substrate.

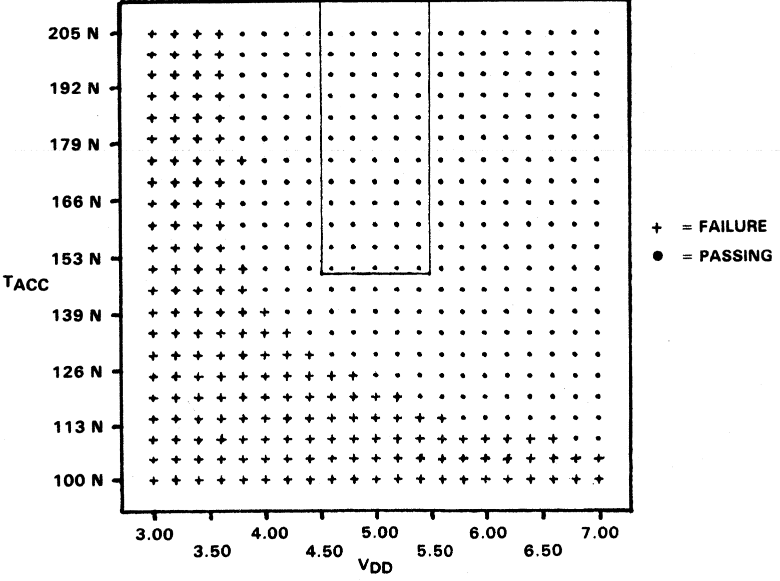


FIGURE 10 – TYPICAL SHMOO PLOT AT 88°C

TABLE 1 – REFRESH TIMES FOR SINGLE CRYSTAL VS. EPITAXIAL SILICON

SINGLE CRYSTAL			EPITAXIAL		
UNIT	BURST (ms)	DISTURB (ms)	UNIT	BURST (ms)	DISTURB (ms)
A	318	6	A	502	92
B	234	4	B	1000	132
C	184	4	C	600	57
D	247	4	D	520	111
E	196	8	E	430	87
F	14	4	F	241	56

NOTE: T_{case} = 90°C.

Enhanced oxide reliability has been accomplished in TMS 4164 wafer fabrication process with the use of lower (relatively) temperature thermal oxidation in a carefully controlled HCL oxidation growth process. Minimizing the exposure of the critical gate insulator to organic/inorganic elements/chemicals prior to highly pure polysilicon deposition enhances the long-term system reliability by reducing time-dependent gate oxide ruptures and mobile ionic contamination presence in a carefully controlled environment. Nominal 3μ poly leads are etched with dry processing techniques to ensure tight physical geometry/electric parameter control. Low phosphorus concentrations in multilevel doped insulator minimizes metal corrosion at high humidity operation. Sputtered silicon-doped aluminum covering smoothly "reflown" oxide steps coupled with low power dissipation (less than 100 milliwatts at system cycle operation) minimizes electromigration and keeps the chip relatively cool.

MULTIPROBE DEVICE TESTING

Before dividing the wafer into individual devices, it is electrically tested via probes. The wafer probe operation is the first functional testing of the memory. This three-fold test accomplishes the following:

(1) Eliminates non-functional devices that, if assembled, would not meet the rigid requirements of back end final test.

(2) Provides the product engineer with actual parametric characteristics that are a function of the front end (fabrication) process. This is accomplished by providing test sites for such transistors, capacitors, continuity and leakage structures. These sites are related to the devices used in memory periphery and array.

(3) Provides characterization of the memory device itself by finding minimum and maximum operating parameters. This is done typically on a sample basis and gives immediate feedback to process/product engineering.

The functional devices from probe are then assembled (see Appendix B) before final testing.

Testing the TMS 4164 has evolved from earlier DRAM testing including the TMS 4116 program. After comprehending additional addresses, the same pattern and data sequences can be applied to the TMS 4164 as were applied to the TMS 4116. However, the device has developed its own characteristics that require customized programs with unique patterns. These test patterns guarantee a quality device while incurring a minimum of test time.

The patterns used in production are those determined from the internal logic and layout to produce the greatest possibility of failure detection. These tests cannot make up a truly comprehensive pattern test of memory array as there are 265,536 possible data patterns. Subsets of these patterns can be located to ensure that pattern sensitivity does not exist in the part, and that certain locations are not unduly susceptible to noise on control, address, or power pins.

The bit map of the TMS 4164 (Figure 11) suggests more testing considerations as the data to one of the two halves of the device array is inverted. The identification of memory failure mode is dependent on this type of information. The test flow and test descriptions are in Appendix C. A bit map of the TMS 4164 can be obtained using the true address bit significance as shown in Figure 11.

When a product is in its infancy, the correlation of final test failures to multiprobe testing is handled differently from the correlation of a mature device. During product development, the product engineer must optimize the total number of devices with little regard for assembly and test costs. As a product reaches maturity, a stringent multiprobe test optimizes final test yields thus reducing back end costs. This becomes important in high-volume production devices, such as DRAMs, where a significant portion of the final cost is directly related to assembly and test yields.

Texas Instruments has the capability for special test flows for those customers who require particular device functionality beyond typical operating parameters. These special test flows may include additional burn-in testing for reduced near-term failure rate or testing for operation outside the normal electrical or temperature range. Each of these flows is assigned a number. Parts passing these tests are given this number in addition to normal device markings.

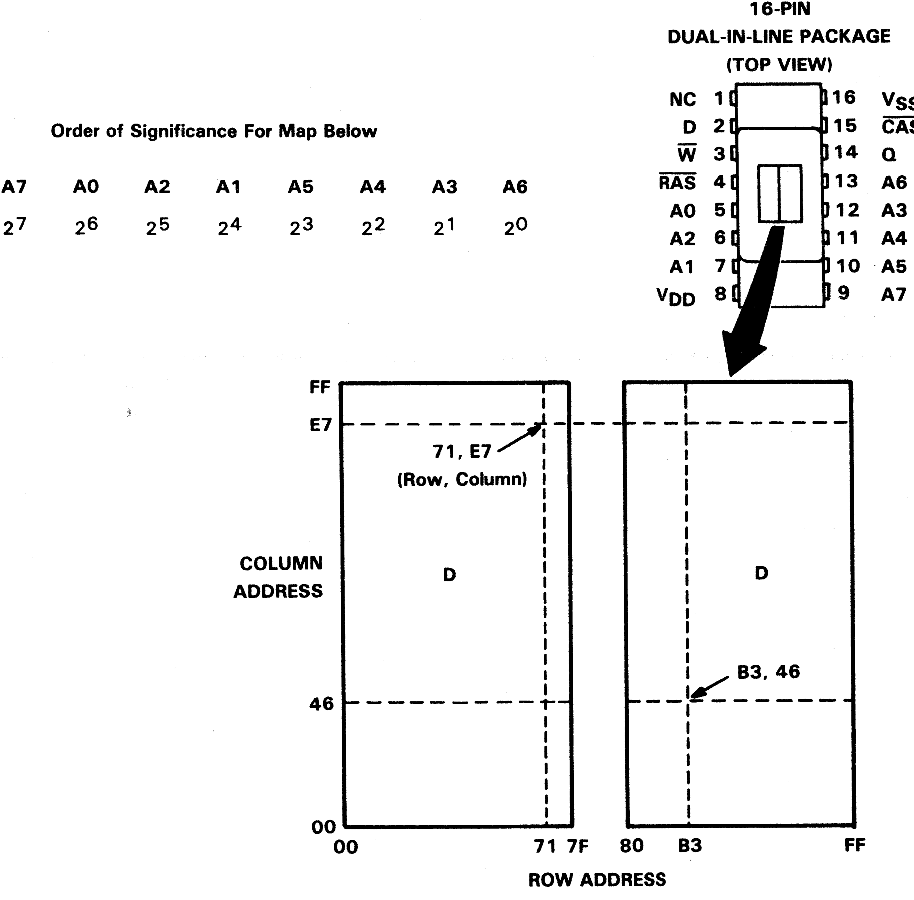


FIGURE 11 – TMS 4164 BIT MAP

Data on the left half of the array (as shown above) is stored in inverted form (1 = absence of charge) while data on the right half is stored in true form (1 = charge). Therefore, row address bit 7 is the bit that selects between the true and inverted array.

TEST EQUIPMENT CALIBRATION

To ensure that the product is tested accurately, a Quality Control (QC) procedure has been established for device testing equipment. This is a special set of diagnostic routines that are unique to the TMS 4164 and are in addition to the normal maintenance of the test equipment. These routines include:

(1) Maximum edge accuracy in all timing signals (This eliminates address skew and insures compare strobe integrity, etc.)

(2) Driver voltage accuracy to insure precise V_{IL} and V_{IH} levels

(3) Power supply accuracy

(4) Handler temperature accuracy

(5) Test contact resistivity, leakage

These diagnostics are performed prior to Quality Assurance (QA) acceptance procedures during each production shift.

QUALITY AND RELIABILITY PROGRAM

INCOMING QA

Just as our customers need quality components to build reliable systems, TI must require that the materials and equipment we use provide the necessary quality to our products. For that purpose Texas Instruments maintains an effective incoming material control on all production material and parts that become a part of or are consumed in the manufacturing process. The tests and evaluations performed include inspections of mechanical, physical, dimensional, functional and electrical characteristics as specified in the TI documents that are supplied to the vendor with the purchase orders. For example, vital to TMS 4164 reliability is the control of mold compounds for the plastic encapsulation process. Texas Instruments maintains strict incoming material control to guarantee proper chemical formulation, molding characteristics and properties of the molded material. A preshipment sample of each lot of mold compound must pass incoming QC before the vendor is allowed to ship the lot. Upon passing incoming inspection, an acceptance number is assigned to the lot of mold compound and communicated to the vendor and to TI molding operations worldwide. In addition, comprehensive material specification and inspection procedures are maintained to assure consistency in moldability and reliability.

MOS QUALITY AND RELIABILITY ASSURANCE (QRA) PROGRAM

The production flow for dynamic RAMs is shown in Appendices A and B. Built-in reliability is guaranteed by stringent process controls, in-line monitors of critical parameters, and rigid acceptance procedures of pieceparts. Various analytical instruments are utilized to monitor processes, trouble-shoot manufacturing process problems, and perform engineering evaluations. This approach assures optimum control of etch times, diffusions, metallization clean-ups, etc. Control charts are maintained on parameters, such as oxide and film thickness, junction depths, topological geometries, and electrical parameters. High temperature and voltage stress samples are evaluated on a skip lot basis. These tests with pre- and post-stress measurements evaluate the process stability and provide control with early corrective action feedback.

SOURCE OF RELIABILITY DATA

Reliability data is collected by following the QRA flow for dynamic RAMs (see Appendix D).

By executing the evaluations in a rigorous and thorough manner current and accurate electrical and mechanical data are obtained. This data indicates the reliability status of the manufacturing processes in an ongoing basis. Analysis of the reject units provides the information for corrective action and continued improvements. New devices, packages, production sites or revised processes are thoroughly tested via the left-hand leg of the flowchart shown in Appendix D. Thus product worthiness is proved before volume commitments are made. As required, additional testing by TI or by the customer may also be performed. Shared data and analysis further adds to the experience base for quality and reliability improvements.

Ensuring that TMS 4164 shipments are of the highest quality and reliability is our primary goal; however, we want our customers to benefit the most from our efforts. Consequently, TI provides customer support after the parts are shipped (see Appendix K). We combine our knowledge of how the devices work with expertise in system design to help customers improve system reliability.

MOS DEVICE ANALYSIS

The importance of quality and reliability improvements are reflected in the number of techniques and amount of resources that are dedicated to this effort. At Texas Instruments these resources have been increased at a very significant rate over the past few years. Recommended procedures in the quality and reliability improvement program are shown in Table 2. Further support in solving the problem and cause is furnished by the failure analysis flow given in Appendix F. This flow not only shows the thought or decision process but also includes the equipment used and a projected cycle time.

TABLE 2 – QUALITY AND RELIABILITY IMPROVEMENT PROCEDURE

The PROBLEM

The problem must be described and quantified in specific terms.

The CAUSE

The cause must be identified and defined as accurately as possible based upon the available information.

SHORT TERM ACTION

Identify the immediate action to be taken to limit the problem and the effective date of the action.

LONG RANGE ACTION

Show the planned action and effective date for permanent problem correction.

VERIFICATION

Measure the effectiveness of the actions by indications that chart problem severity. Actions are not considered complete until indicators show effective resolution.

OUTLOOK

Project the long range effect of the problem and corrective actions. State the degree of confidence in the effectiveness of the actions.

COST

Account for total cost of corrections.

ELECTROSTATIC DISCHARGE TESTING

Occasionally special testing is done to comply with specific requirements of the customer. An example of this testing service is described next.

Tests have been performed on 30 TMS 4164 parts to determine the effects of various levels of electrostatic discharge on the functionality of the devices. The 30 units were tested in three groups of 10 units each. Group #1 was tested with increasingly positive electrostatic discharge voltage (V_{ESD}). Group #2 with increasingly negative V_{ESD}. Group #3 was further separated into five subgroups of two and each of these was repetitively tested at a different V_{ESD}.

Testing consisted of applying a 150 pF capacitor charged to a specific V_{ESD} ranging from ±400 to 700 volts through a 2.2KΩ resistor to the pin under test (PUT). All voltages and currents were referenced to pin #16 (V_{SS}). PUT was then checked for leakage and continuity. A pin failed the leakage test if the current exceeded 10 microamperes when −5.5 volts was applied. PUT failed the continuity test if it required more than +1.5 volts to force 80 microamperes into it.

Each device in Group #1 was tested at 400, 450, 500, 600, 700 volts. The devices in Group #2 were tested in the same manner but using negative voltages. Each subgroup of Group #3 was tested 20 times at one of the following V_{ESD}s: 450, 500, 550, 600, 700 volts. Once any given PUT failed, it was skipped in succeeding test repetitions.

The results are tabulated below:

TABLE 3 – NUMBER OF PIN FAILURES

GROUP #	TYPE OF FAILURE	700 V	600 V	550 V	500 V	450V	400 V
1.	CONTY	8	3	0	0	0	0
	LEAKAGE	8	0	0	0	0	0
2.†	CONTY	33	6	3	0	0	0
	LEAKAGE	3	1	0	0	0	0
3‡	CONTY	20	20	23	11	0	–
	LEAKAGE	4	2	0	0	0	–

† Negative V_{ESD}
‡ Repeat 20 times or until failure

ELECTROSTATIC DISCHARGE TESTING ON IMPROVED INPUTS

Improved input protection circuits have been subjected to electrostatic discharge testing which indicate that the circuit will withstand ESD voltages greater than 2000 volts. The improved input protection circuit shown in Figure 11A will be implemented on the TMS 4164A and the TMS 4416 in late 1982.

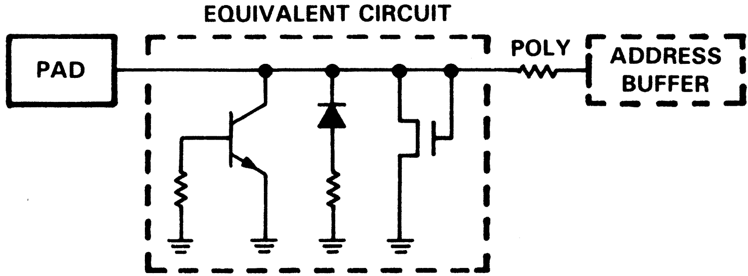


FIGURE 11A – 0.8 MIL SQUARE DIODE AND 50/3 MICRON METAL GATE FIELD TRANSISTOR

Testing consisted of applying a 150 pF capacitor that was charged to a specific V_{ESD} from ± 500 volts to > ± 4000 volts through a 1.5KΩ resistor to the pin under test (PUT). All voltages and currents were referenced to pin 16 (V_{SS}). PUT was then checked for leakage and continuity. A pin failed the leakage test if the current exceeded 1 microampere when – 5 volts was applied. PUT failed the continuity test if it required more than + 1.5 volts to force 80 microamperes into it.

MOS QRA LIFE TEST SUMMARY

Accelerated life testing is performed routinely on random samples of prototype and production units. Shown below is a summary of all life testing on plastic parts for the first three quarters of 1982.

TEST °C	QTY	REJ	ACTUAL DEV HRS	DEV HRS @ 55 °C	FITS* 60% UCL
125	5,419	35	4,861,700	109,000,000	341

* FITs or Failures in Test reflect the number of failures in 10^9 device hours (1 FIT = 1 failure per 10^9 device-hour).

MOSFET OPERATION

An N-channel enhancement-mode MOSFET is illustrated in Figure 12. The three terminals identified are the source (reference terminal), the gate (control electrode), and the drain or device output. These terminals may be roughly compared to the bipolar's emitter, base, and collector. With the substrate source and gate grounded, and the drain held at some positive potential, the reverse biased drain-to-substrate PN junction prevents drain-to-source current flow.

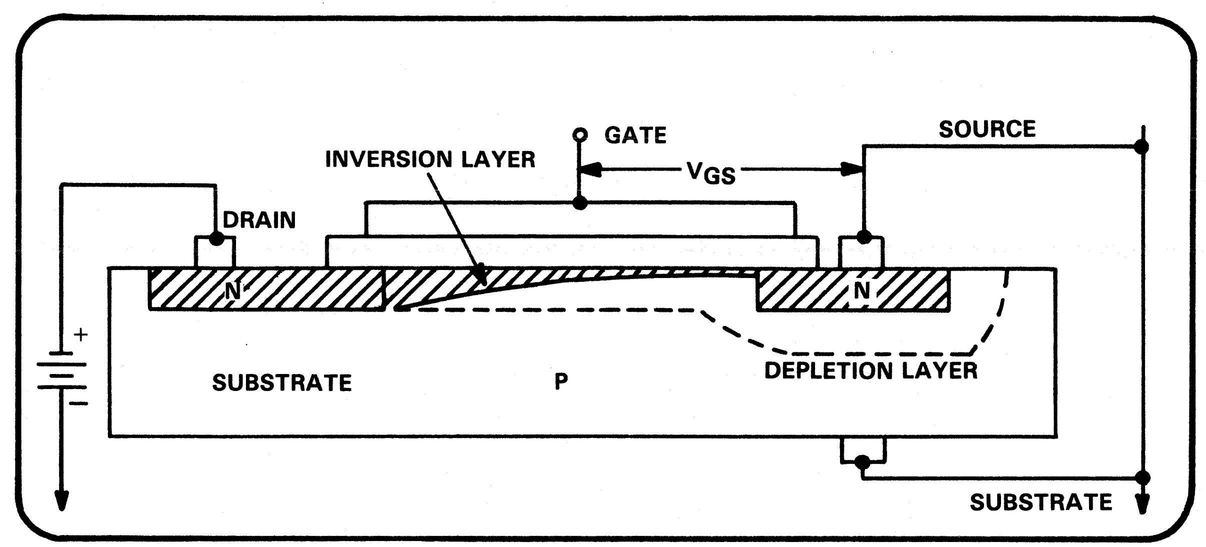


FIGURE 12 – N-CHANNEL ENHANCEMENT MODE MOSFET

The gate electrode controls charge in the substrate "channel" between source and drain. When a negative voltage (with respect to the source) is applied to the gate terminal, free electrons in the silicon substrate between drain and source are repelled forming an accumulation region of holes. Positive bias attracts electrons to this region until an inversion layer or a negative conductive channel between N-type source and drain forms. The voltage required at the terminal to form channel inversion is referred to as threshold voltage of V_T.

Since source and drain are virtually interchangeable, channel current can flow in either direction. The MOSFET, therefore, becomes an ideal switch, capable of bilateral current flow with an almost infinite off impedance.

A few additional words should be included here concerning MOS capacitance. The input terminal of the MOSFET, in combination with the gate-oxide insulator and silicon substrate, form a voltage-dependent capacitor. This gate capacitance is particularly important for in-process studies of oxide-layer properties, e.g., contamination in the oxide and its effects on the oxide-silicon surface characteristics. Threshold voltage and oxide properties are vital to understanding MOS failure mechanisms.

WHAT IS FAILURE?

A device failure is defined as the cessation of ability to perform a specified function or functions within previously established limits. This requires that measurable limits be defined to describe satisfactory performance. Most users are concerned with the overall performance of the system in the hands of the ultimate consumer. Small shifts in device parameters are possible, but these are usually insignificant and do not contribute to degraded performance at the system level. While the designer has control over a conservative system design, he must anticipate the intended working environment.

FUNCTIONAL VERSUS PARAMETRIC

A functional failure may be one that is termed catastrophic or totally non-operable or one that lacks at least some degree of functionality. The functional failure may be either chip or package-related but is usually the result of a manufacturing defect or improper use in the hands of a customer. Parametric failures are those that involve an electric parameter or parameters that no longer meet a guaranteed data sheet limit. In many cases these "failures" will continue to function properly in a well-designed system. Parametric failures are usually chip-related or involve an interaction of package and chip. Diffusion leakage, MOS surface leakage currents, and shifts in threshold voltages are all examples of failure modes that may contribute to parametric failures. These effects may manifest themselves as input/output leakages, reduced drive capability, skewed oscillator frequencies, etc. The primary concern of parametrics is the indication of a processing problem that may degrade with time to a functional failure as defined by system requirements. All semiconductor products will experience certain changes in electrical parameters with time. It is only those showing a rapid shift to "out of spec" tolerances that concern the component reliability engineer and system user.

MOS FAILURE MECHANISMS

MOS memory failures that occur after comprehensive electrical testing result mostly from processing flaws that exist in the chip or package. Chip-processing related defects control the failure rate in the case of the TMS 4164. Because of this, it is necessary to understand and control the MOS chip-processing facilities and variables critical to reliability. Included below is a brief summary of failure mechanisms that can contribute to reduced MOS product reliability.

CHIP-PROCESS RELATED MECHANISMS

Mobile Ions (Parametric Drift). All oxides are sensitive to ionic contamination, which will migrate in the oxide under electrical and thermal stress. The predominant effect of excessive contamination in gate oxides is a shift in the threshold voltage after application of voltage and temperature. Under such conditions, negative gate voltages attract positive charge to the gate electrode and drive negative charge to the oxide-silicon interface.

Electrochemical Corrosion. The corrosion of aluminum metallization may be caused by excessive moisture penetration and/or residual chemicals on the chip surface. This is manifested by high-impedance leakage, an open connection, or loss of ohmic contact. Attention to cleanliness, packaging materials, and the packaging process control reduces this hazard.

Metal Cracks. Improper oxide contours resulting from incorrect thickness or procedure allow a thinning of metallization and cracking at extreme steps. A Scanning Electron Microscope metallization monitor controls the process for out-of-tolerance aluminum coverage.

Oxide Defects. Oxide defects in the gate and field insulators can be particularly troublesome to device operation. These defects are categorized by pinholes, scratches, and undercutting. A pinhole is an isolated region where the dielectric has broken down. When this occurs, a short to the silicon substrate is created. Scratches in field oxide may result in incomplete diffusion masking during later stages of processing. Oxide undercutting results in an increase in dimensions of an oxide window during oxide removal. When excessive, this can lead to latent failure modes. The utmost care and control of oxide operations is necessary to guarantee high reliability since these areas are some of the most critical to long-term device performance.

Inversion (Spurious MOSFET Leakage). Since turn-on voltages of most MOSFETs in application are dependent upon the potentials of source and drain as well as the inherent V_T of the device, it is frequently necessary to apply gate voltages well above the device V_T. Under certain conditions this voltage is sufficient to cause inversion under thick-field oxides resulting in the establishment of current paths between N-type diffusions and loss of isolation. This problem can be caused by thin field oxide or decreased oxide charge associated with the thick oxide. These effects are also created by lateral charge spreading from high-voltage nodes along the surface of the field oxide. A process control technique has been developed to detect lateral charge spreading tendencies in lots where insufficent cleanups allow ionic contaminants to migrate and form unwanted field inversions.

Diffusion Leakage. Diode leakage can result from irregular oxide photoengraving prior to source-drain diffusion resulting in irregular diffusion profiles. Defects in the starting silicon material, if located in the depletion region of source or drain diffusions, may also cause anomalies in diode characteristics. Careful slice handling and the avoidance of extreme temperatures during processing contribute to the decreased defect levels in substrate silicon.

Thermocompression Bonding Failures. The gold-aluminum bonding system employed in MOS processing is subject to formation of gold-aluminum intermetallics and voiding when subjected to uncontrolled high temperatures. This voiding, if severe, can lead to high-resistance bonds and ultimately to lifted bond wires. The formation of these compounds has been minimized by using strict temperature controls during fabrication and by limiting operating temperature to 125 °C or less and storage temperature to 150 °C.

Header/Materials Failures. Package failures can result from faults with the ceramic header or lead frame. Poor plating can result in lifted bonds at the post. Open metallization within the ceramic header can cause lack of continuity to the bar and result in electrical failure. If the plastic encapsulation material processes are not properly controlled, failure can result after exposure to the intended environment. Improper coefficients of expansion and contraction can cause lifted or broken bond wires after extended thermal cycle. A high content of mobile ionic contamination in the plastic can create MOS surface leakage problems or contribute to aluminum corrosion tendencies when exposed to high humidity environments. TI has devoted significant resources to develop the proper plastic for MOS use and maintains stringent controls on incoming materials and the encapsulation process.

Chip Damage. Chip cracking can occur during the assembly process and result in latent failures. The cracking may occur around the periphery of the chip, through the active area of the circuitry, or emanate from the bond pads. Cracks around the periphery may be induced during scribe and break. These cracks may propagate to areas of active circuitry after exposure to later processing stresses. Cracks radiating from bonding pads result from thermal or mechanical stresses induced during thermocompression ball bonding. Bond pad cracks can be a threat to reliability since they may be concealed by ball bond and bonding pad.

FAILURE RATE CALCULATION

An understanding of the reliability capabilities of a system in terms meaningful to the user requires a basic knowledge of component and system failure rate calculations and the treatment of accelerated test data.

Suppose the cumulative distribution of the life of a given item is Q(t). In other words, the probability that an item will have a life of t or longer is 1-Q(t). This survival probability is called the reliability, designated by R(t) = 1-Q(t). If an item has survived for a time t, the probability it will fail in the next t time units is

$$Q(t+\Delta t) - Q(t) = [1-R(t+\Delta t) - (1-R(t))]$$

$$= -R(t+\Delta t) - R(t)$$

If we take

$$\lim_{\Delta t \to 0} - \Sigma \frac{[R(t+\Delta t) - R(t)]}{\Delta t} = \frac{dQ(t)}{dt} = q(t)$$

we get the density function of the distribution of life Q(t):i.e.,

$$\frac{dR(t)}{dt} = -q(t) \bullet$$

If we divide q(t) by R(t), we get the "instantaneous failure rate" or "hazard rate". Therefore, if one started with N items, all operating under identical conditions, then by the time t, we would have on the average NR(t) left. During the next time interval, Δ t, there would, on the average, be

$$\frac{dQ(t)\Delta t}{dt} = -\frac{dR(t)\Delta t}{dt}$$

failures and the failure rate or number of failures during Δt per number of survivals at time t is

$$\frac{-dR}{dt} \frac{\Delta t}{R(t)} \bullet$$

This is the instantaneous failure or hazard rate λ(t)

$$\lambda(t) = \frac{-1}{R(t)} \frac{dR(t)}{dt} = \frac{q(t)}{R(t)} \bullet$$

The reliability function is then given by:

$$R(t) = Ke^{-\int_0^t \lambda(t)dt}$$

where K is a proportionality constant.

If $\lambda(t)$ is assumed constant, then

$$R(t) = Ke^{-\lambda(t)}$$

and the failure rate is described by device failures occurring randomly in time. It is well known that semiconductors typically follow a "bathtub" curve in the infant mortality and constant failure rate regions when failure rate is plotted versus time. Wearout is not normally observed in system use but can be produced by highly accelerated testing techniques. This is shown in Figure 13.

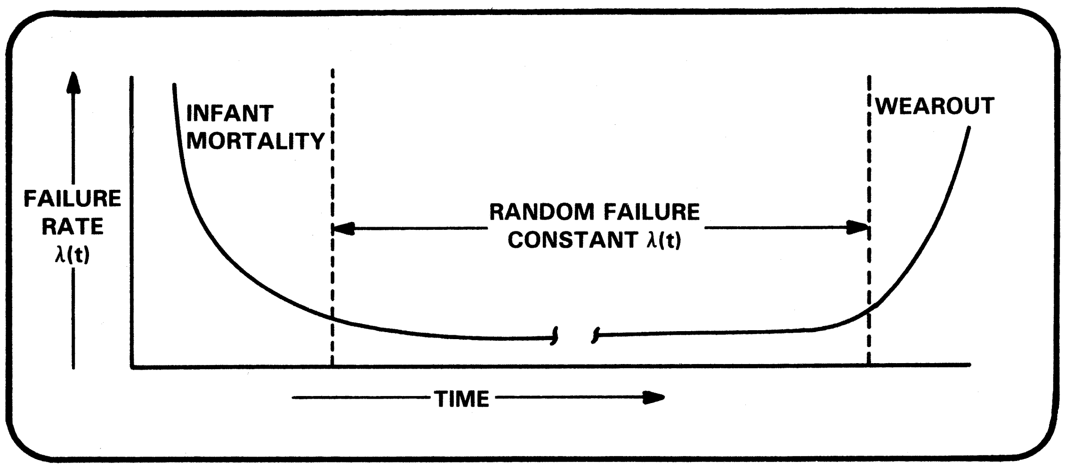


FIGURE 13 – CHARACTERISTIC CURVE COMPONENT LIFE

The infant mortality portion of this curve defines the time during which a portion of the product containing manufacturing defects fails at excessive levels. These "freak failures" are superimposed on the normal life distribution and, when properly screened, are not expected during the normal life of a product at use condition. The random failure portion of the failure rate curve is the expected use condition time period during which those devices that are reliability hazards will fail predictably. The onset of wearout is defined by an increasing failure rate with time and is depicted by an upturn portion of the bathtub curve. It is clear that the useful life of a TMS 4164 is described by the random failure portion of the bathtub curve. The infant mortality occurs very early in life and the mechanisms within this time frame are frequently temperature-accelerated. The constant failure rate period is known as the useful life. A burn-in or run-in at the device or board/system level will aid in removing infant mortality. The cost of this operation must be weighed against the advantages of failure rate improvement and the reliability needs of the system. Several time-dependent models, including the Weibull and log-normal distribution, have been used to treat the time-varying failure rate.

Next to consider is a constant failure rate estimate after infant mortality removal with comments on preconditioning and its impact.

Extensive accelerated testing has been performed on the TMS 4164 process to define the failure rate distribution with associated failure mechanisms and to predict expected use condition reliability performance in time. Multi-temperature life tests are performed routinely on TMS 4164 series product line. The effect of temperature on failure rate is determined using the classical Arrhenius reaction rate model as it applies to semiconductor failure mechanisms.

The reaction rate constant is given as:

$$K = A_e^{-E/k_BT}$$

where k_B is Boltzman's constant (8.63×10^{-5}eV/°K); A is a proportionality constant; E is the activation energy; and T is the absolute temperature. The life of a TMS 4164 is assumed to begin at the initiation (by some applied stress) of the reactions that occur on/in the chip and degrade device performance. Hence one may write:

$$\lambda \propto e^{-E/k_B T}$$

and plot the failure rate vs. 1/T to determine the activation energy for the failure mode of interest. From this information the acceleration factor (A.F.) between any two temperatures (T_1 and T_2) may be calculated from:

$$\frac{\lambda_2}{\lambda_1} = \text{A.F.} = e^{(E/K_B) \times [(T_2 - T_1)/T_2 T_1]}$$

Included in Figures 14 and 15 are a series of curves generated from the acceleration factor expression that allow rapid approximation of acceleration factors for given activation energies. These curves can be used to estimate acceleration to be anticipated over various temperature ranges for the observed activation energy of any component. Of course, only after testing at various temperatures can the activation be determined. It can readily be seen that small changes in activation energy greatly affect the derating-to-use condition temperatures.

The overall TMS 4164 MOS process is characterized by a temperature activation energy of 0.5 eV for a composite of failure mechanisms, which is considered to be an extremely conservative figure. Device level testing in energized sockets at nominal voltages and at temperatures ranging from 35 °C to 125 °C are performed routinely to provide failure rate and activation information. Accelerated package testing is also conducted.

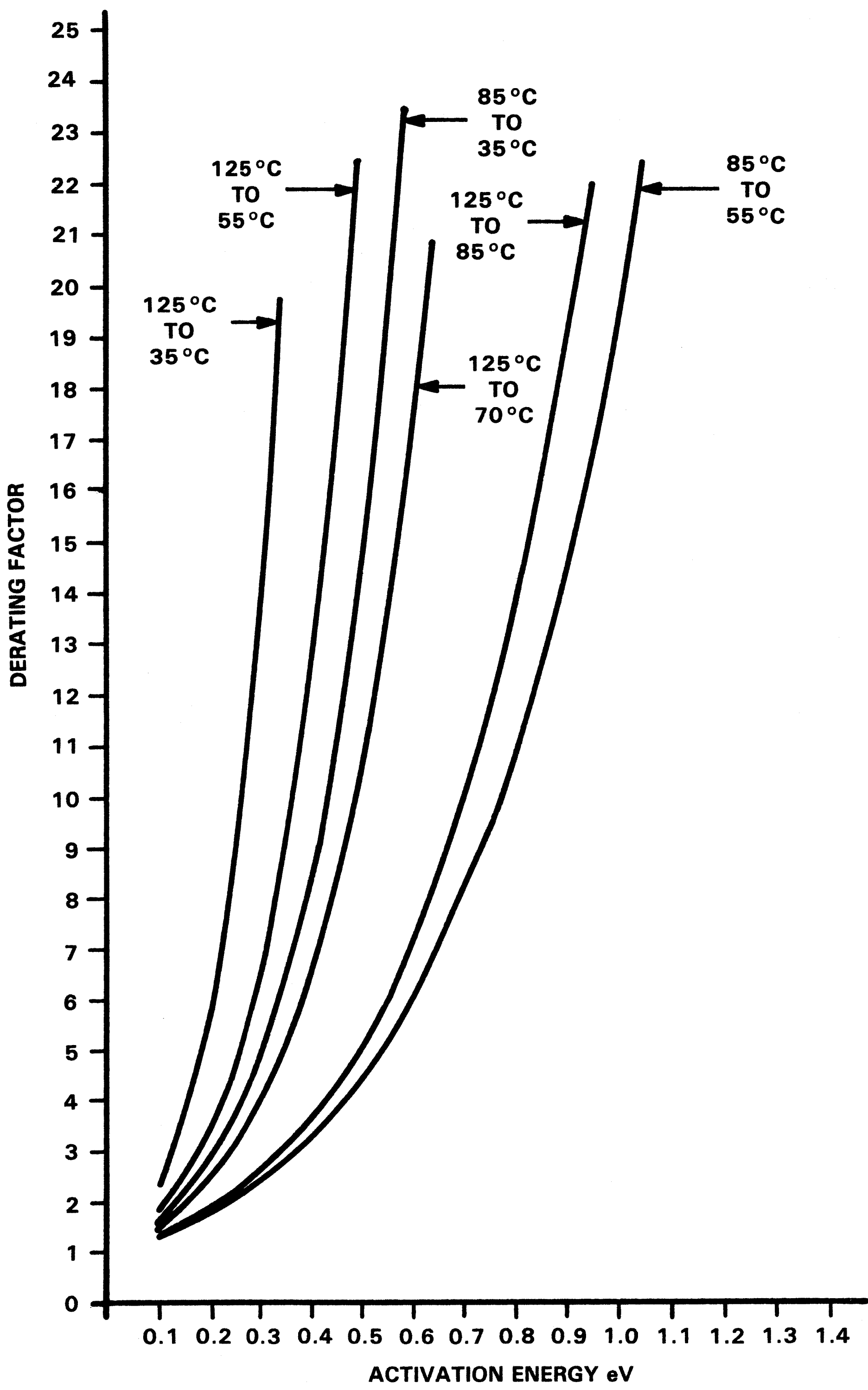


FIGURE 14 – DERATING FACTORS FOR VARIOUS ACTIVATION ENERGIES

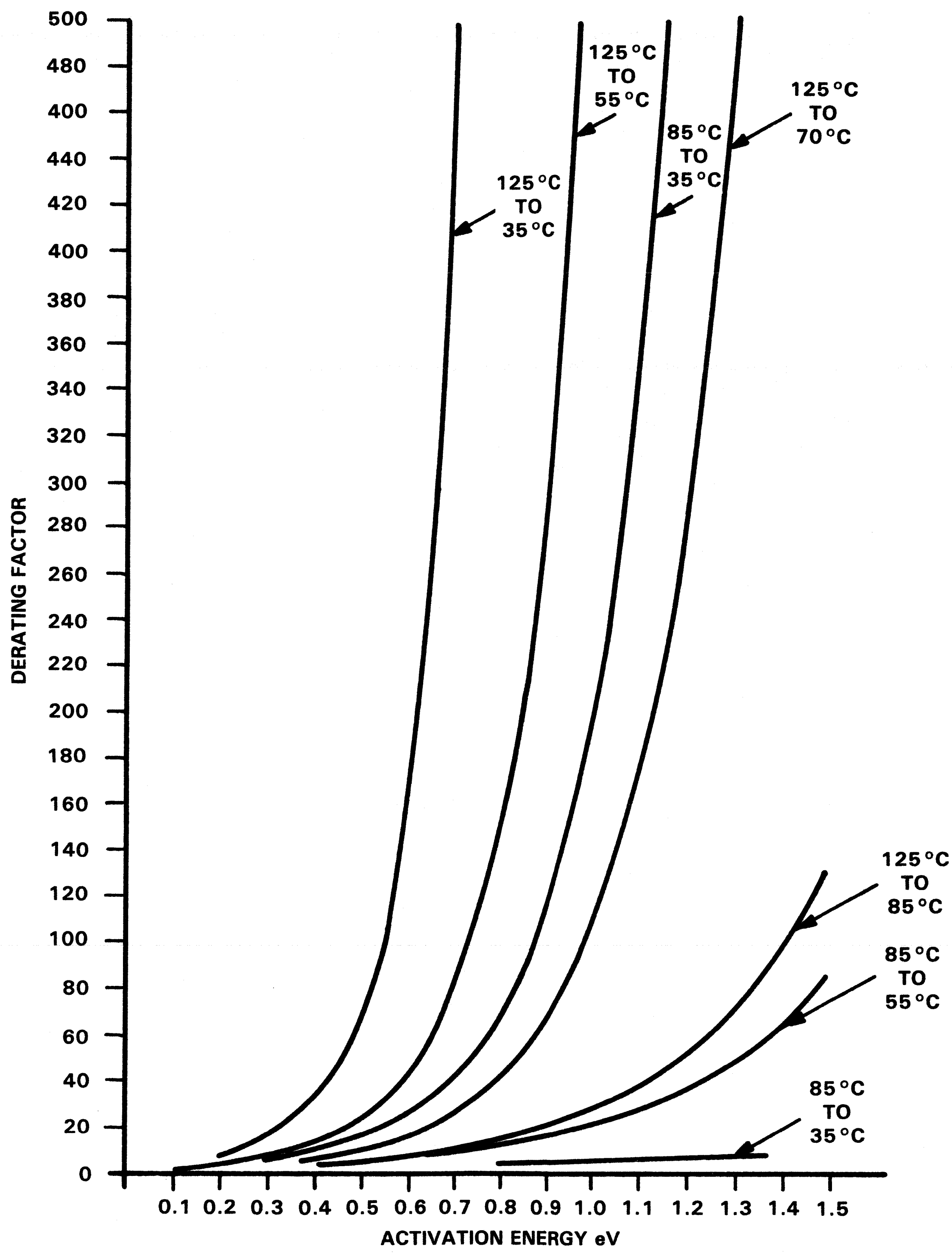


FIGURE 15 – HIGHER DERATING FACTORS FOR ACTIVATION ENERGIES

TEST FACILITIES

The people and equipment resources to implement the above procedure and flow represent considerable investment. Organization of the QRA laboratories in Houston, for instance, is shown in the chart in Appendix E. This organization primarily supports the analytical work on finished products and also services the Houston Diffusion Facilities. Similar facilities exist in Dallas, Lubbock, and Singapore to provide site support. The major equipment in the Houston laboratories is shown in the following illustrations. For initial failure analysis work, the Automatic Memory Tester, shown in Figure 16, coupled to a probe station exercises the questionable circuit. After analysis to determine failure symptoms, the Manual Probe Station (Figure 17) is used for internal probing to find the failed point. Further analysis must be done on a level-by-level basis, with emphasis on topology and chemical nature of the defect. Figure 18 shows a Scanning Electron Microscope coupled to an Energy Dispersion X-ray. Figure 19 is that of a Scanning Auger Microscope capable of examining the top 10-20 angstroms of an integrated circuit to indicate a chemical profile.

Peripheral support equipment within the laboratory includes complete chemical facilities for decapsulating plastic devices, delaminating chips to reveal defects, and performing various etching techniques including dry plasma etching. Also available are optical microscopy with photographic and mechanical screening capabilities. Since even simple current leakage problems may show up only under particular operating conditions, large scale integrated circuits, like the DRAM family, require advanced methods including scanning electron microscopy.

Several years of analysis of silicon-gate devices have contributed to a detailed understanding of the mechanisms that characterize the N-MOS process and DRAMS. The Device Analysis Laboratory at TI is the primary means for determining the physical cause of reliability hazards and proper corrective action by design, chip fabrication, or assembly processing staffs.

FIGURE 16 – AUTOMATIC MEMORY TESTER

FIGURE 17 – MANUAL PROBE STATION

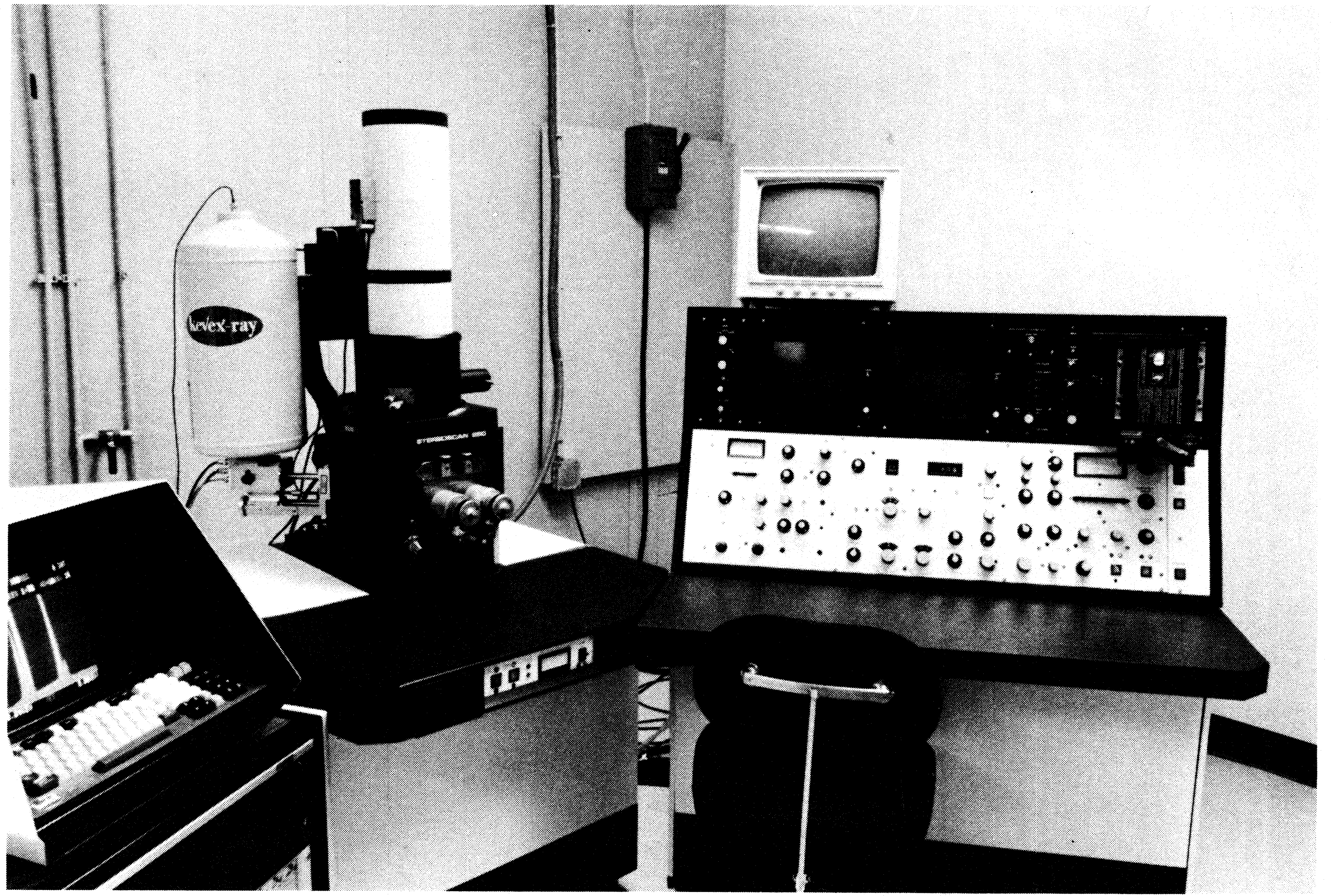


FIGURE 18 – SCANNING ELECTRON MICROSCOPE

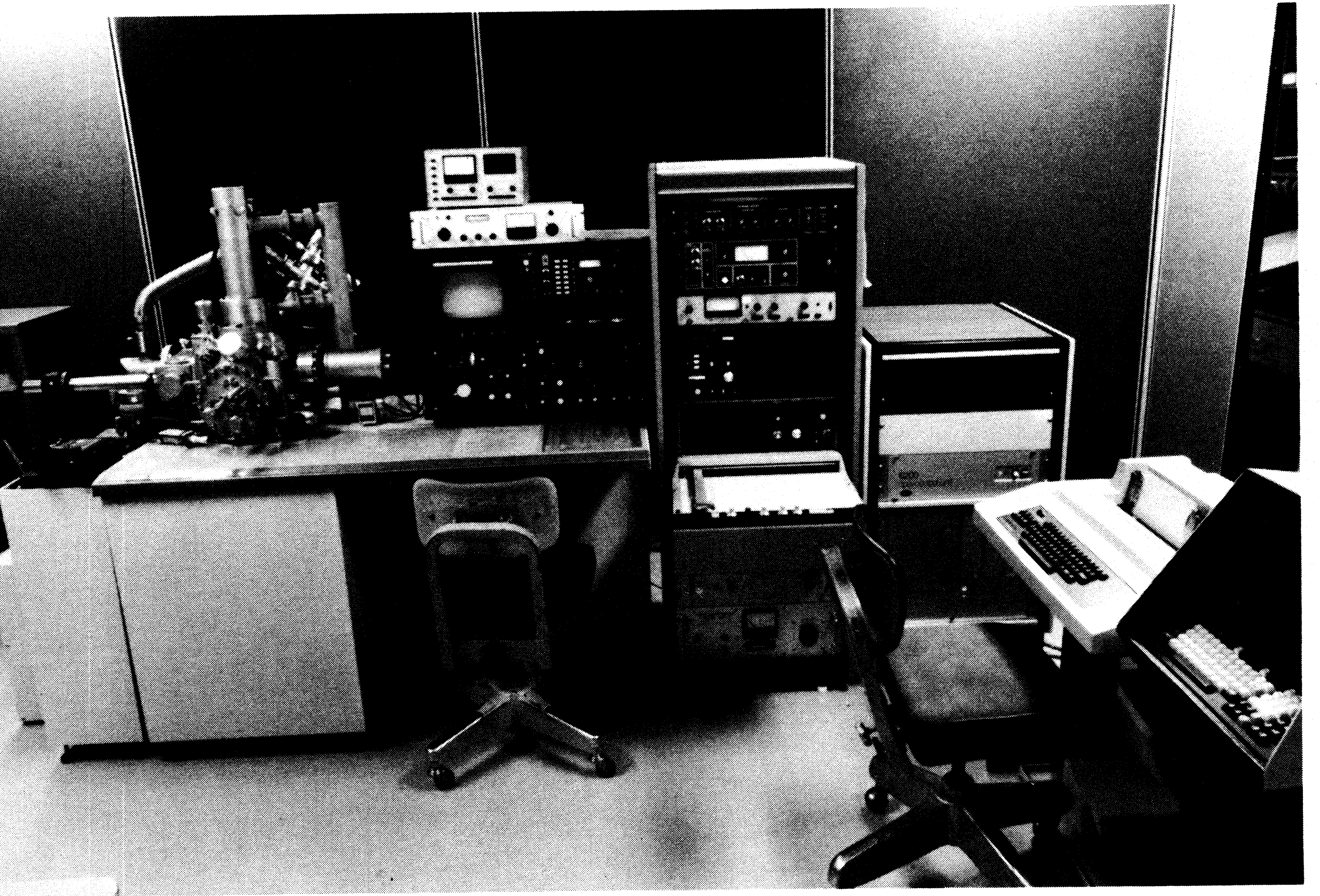


FIGURE 19 – SCANNING AUGER MICROPROBE

ALPHA PARTICLE CASE

THE PROBLEM

Since 1978, when alpha particles were found to be responsible for the generation of soft errors in memories, much work has been done to minimize the sensitivity of parts to these particles. The problem arises as geometries of new VLSI circuits reach dimensions that are affected by atomic events. The primary source of alpha particles causing soft errors is the decay of the trace amounts of uranium and thorium located in packaging materials for DRAMs.

Solutions to the soft error problem are being sought in these areas at TI:

(1) Reduced package emissions

(2) Shielding the device

(3) Employing new processes and design techniques

Figure 20 shows the relative reductions made in alpha emissions in ceramic packages since 1978. These reductions show a 200X improvement.

Adoption of the shielding approach has been announced by all manufacturers of 64K DRAMs. The type of shield varies but the end result is the same – adding a suitable thickness of material to the top of the chip to ensure alpha particles do not reach the active area of the device. This "overcoat" must be selected to have a low alpha emission rate, not cause any mechanical failures, not react chemically with the device, and be capable of withstanding processing.

THE SOLUTION

Twenty overcoat materials and processes were tested to find the best one for the 64K DRAM. Some materials broke wire bonds on temperature cycling; some would not take ceramic sealing temperature without decomposing; some became a source for ionic contamination; some caused moisture problems; some required elaborate schemes for application. The material finally chosen was subjected to rigorous quality and reliability tests. As a result, TI is now using single sided polymide tape on plastic devices and a potted polymide overcoat on ceramic units as shown in Figure 21.

Table 4 shows results of the initial alpha shield qualification tests. These tests were made with TMS 4164 as the test vehicle to insure that no compatibility problems were being overlooked.

The sensitivity of the 64K DRAM to errors/min versus cycle time is shown in Figure 22. Using the alpha tester (see Appendix I), the curves were generated with decapsulated units and an alpha source located above the device. These curves illustrate a dependence on cycle time, indicating the alpha particles were causing errors due to hits on the bit lines. The flattening of the "true ones" curve shows the region where alpha hits on the cell became the predominant failure mode. Reduction in alpha sensitivity can thus be seen in Table 5 where errors in uncoated parts are compared to errors in overcoated parts.

TABLE 4 – ALPHA SHIELD QUALIFICATION TESTS

GROUP	ENVIRONMENT	QUANTITY	CONDITION	RESULT
1	125°C Op Life	85	3000 Hour	2 Fail
2	T_{Cy} 65°/150°C	50	1000 Cy	0 Fail
3	Bond Strength	12	2011 Cy	0 Fail
4	Centrifuge/T_{Cy}	50	1000 Cy 2001E	1 Fail
5	Intercavity Moisture	6	Max 5000 ppm	Hi = 1691 ppm Lo = 822 ppm Av = 1034 ppm sigma = 297 ppm

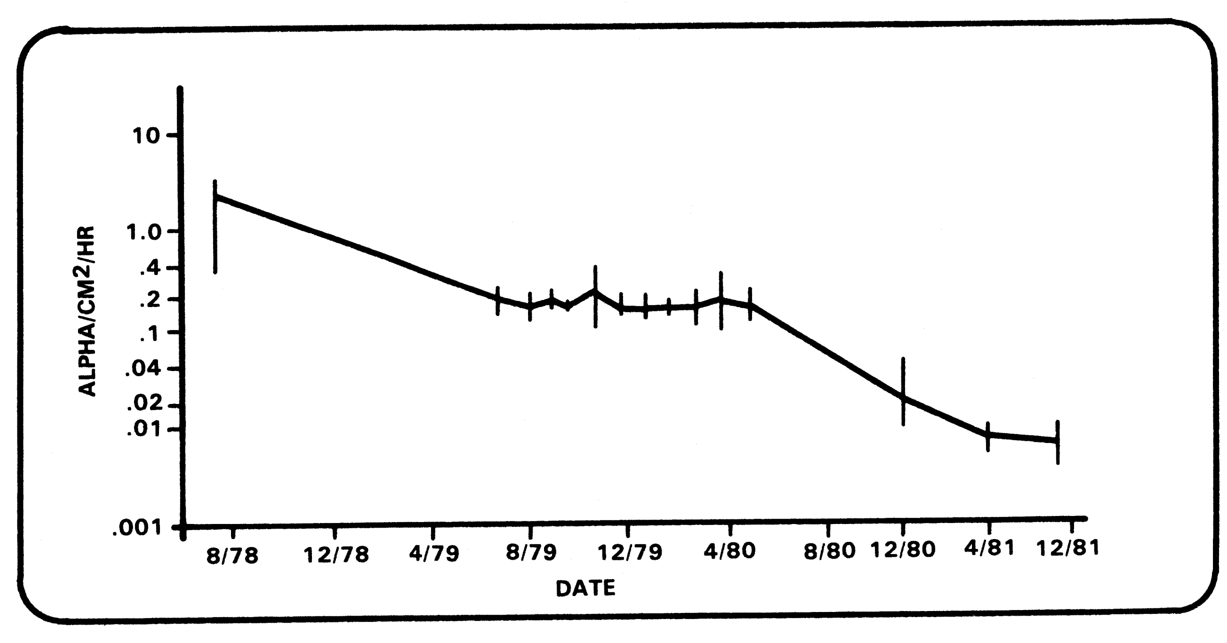


FIGURE 20 – ALPHA EMISSIONS REDUCTION

FIGURE 21 — TMS 4164 WITH PIQ OVERCOAT

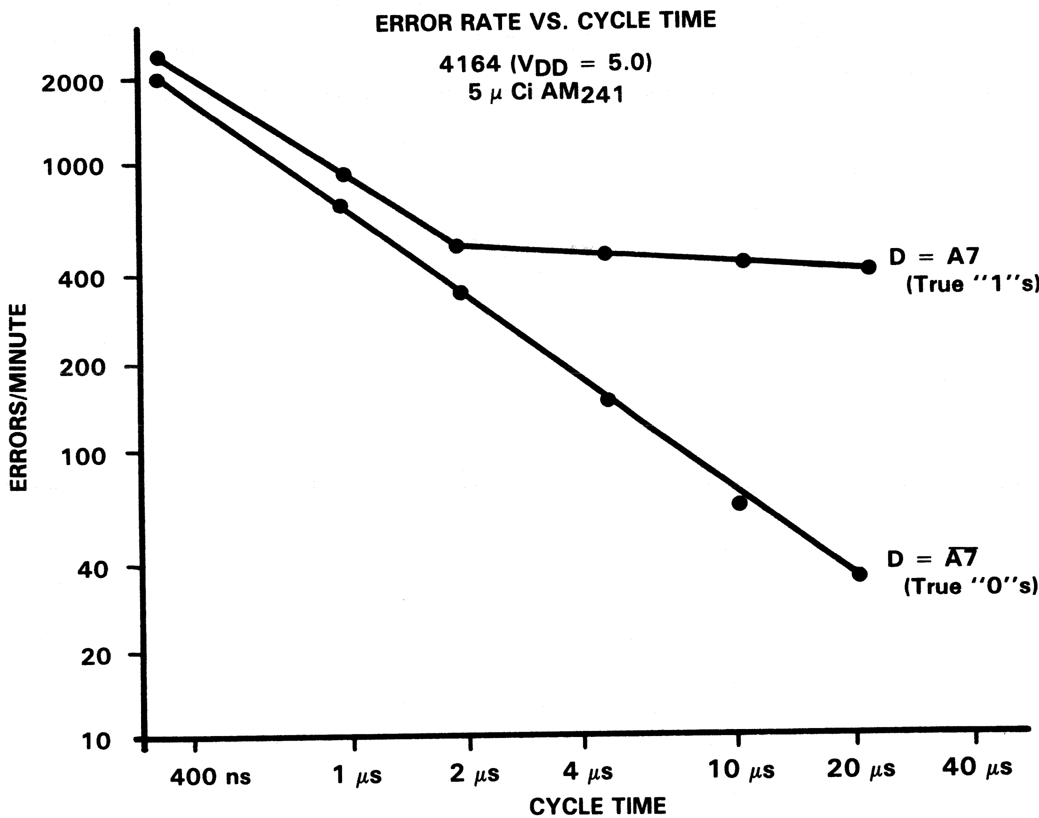


FIGURE 22 – TMS 4164 ERROR RATE VERSUS CYCLE TIME

Below are the results of the accelerated alpha error tests performed on a random sample of TMS 4164 coated and uncoated parts. The tests were performed on an alpha test jig outlined in Appendix I.

TABLE 5 – ERROR COMPARISON

(1) Source: 5 μCi Am_{241}				
	ERRORS PER MINUTE OVERCOATED (Test Duration = 20 min)		ERRORS PER MINUTE UNCOATED (Test Duration = 5 min)	
	Cycle Time		Cycle Time	
	500 ns	5 μs	500 ns	5 μs
1.	0	0	5661	1615
2.	0	0	6268	1695
3.	0	0	4799	804
4.	0	0	6099	1279
5.	0	0	5897	1082
A*	0	0		
B*	0	0		
C*	0	0		
D*	0	0		
(2) Source: 1.9 μCi Th_{228}				
	ERRORS PER MINUTE OVERCOATED (Test Duration = 5 min)		ERRORS PER MINUTE UNCOATED (Test Duration = 5 min)	
	Cycle Time		Cycle Time	
	500 ns	5 μs	500 ns	5 μs
1.	3	2	6115	1587
2.	5	4	5976	1493
3.	5	3	5702	1479
4.	5	4	7075	1836
5.	2	1	7428	2208
(3) Source: 100 μCi Cm_{244}				
	ERRORS PER MINUTE OVERCOATED (Test Duration = 30 min)		ERRORS PER MINUTE UNCOATED (Test Duration = 5 min)	
	Cycle Time		Cycle Time	
	500 ns		500 ns	
E	0		464,000	
F	0		522,000	

* Test duration = 72 hours.

It would appear from the above data that the PIX overcoat effectively eliminates nearly all errors due to radiation originating outside of the overcoat. The only source of vulnerability then, is the overcoat itself. The emission rate of the PIX has been found to be 40 alpha/$cm^2/10^6$ hr. From this we can calculate the number of alpha particles emitted on a coated TMS 4164 as:

#alpha/10^6 hr./device = emission rate of PIX $\times$ area of TMS 4164†

$$= \frac{40\,\alpha}{cm^2 \times 10^6\,hr} \times \frac{3.5 \times 10^4\,mil^2}{device} \times \frac{6.45 \times 10^{-6}\,cm^2}{mil^2} = \frac{9.03\,\alpha}{10^6\,device\text{ - }hr.}$$

Now if we take the results of the test using the 5μCi Am_{241} source, we find that the average number of errors induced per alpha particle emission is (given that 1 μCi of radioactive substance emits 3.7×10^4 alpha particles per second),

† Note that the Th_{228} source emits alpha particles at a higher energy range than found naturally.

$$\frac{\#\,\text{error}}{\alpha} = \frac{\#\,\text{errors/min (due to 5 } \mu\text{Ci AM}_{241})}{\#\,\alpha\text{/min (due to 5 } \mu\text{Ci AM}_{241})}$$

$$= \frac{5545 \text{ error/min}}{5\,\mu\text{Ci} \times \left(\frac{3.7 \times 10^{4}\,\alpha/\text{sec}}{\mu\text{Ci}}\right) \times \frac{60 \text{ sec}}{\text{min}}}$$

$$= 5.0 \times 10^{-4} \text{ errors}/\alpha$$

From here we simply multiply these two results to obtain #errors per 10^9 device – hours, or FITs:

$$\#\,\text{FITs} = \frac{\#\,\alpha}{\text{device hrs}} \times \frac{\#\,\text{errors}}{\alpha}$$

$$= \frac{9.03\,\alpha}{10^{6}\text{ device hrs}} = \frac{5.0 \times 10^{-4}\text{ errors}}{\alpha}$$

$$= \frac{4.5\text{ errors}}{10^{9}\text{ device - hrs.}} \quad \text{or } 4.5 \text{ FITs}$$

These calculations, however, fail to include the effects of high energy particles present in the atmosphere due to cosmic radiation. These high energy particles cannot be adequately shielded (approximately 600 meters of concrete would be required) so their effects must be considered. Calculating the probability of an upset based on the density of radiation is not within the scope of this report; however, the effects are expected to account for the majority of the soft errors experienced.

TI has also established several design innovations that reduce the alpha sensitivity of the TMS 4164. Among these are (1) an EPI layer that decreases the collection depth of the charges generated by alpha particle hits, (2) reduced gate oxide thickness that increases cell capacitance while decreasing cell area, and (3) grounded substrate that reduces the effects of noise on the DRAM.

To monitor the actual soft error rate of the TMS 4164, a memory system tester (MST) was developed (see Appendix J). Results of testing with the MST are updated on a regular basis to reflect new advances in packaging and overcoat materials and to maintain an account base for the errors that impact system reliability.

Based on the results of these tests on TMS 4164 PIX coated parts, representing over 5 million device hours, the soft failure rate is better than 300 FITs and the hard failure rate is 70 FITs. The soft and hard failure rates are specified as 500 FITs and 200 FITs respectively. The MTBF based on these values is shown in the table below.

TABLE 6 – MEAN TIME BETWEEN FAILURES

MEMORY SIZE	SOFT	HARD
64 kilobytes (8 devices)	28.5 years	71.3 years
256 kilobytes (32 devices)	71 years	17.8 years
1024 kilobytes (128 devices)	1.8 years	4.5 years
4096 kilobytes (512 devices)	163 days	407 days

As a practical example, the failure rates and MTBFs for a hypothetical system have been calculated and tabulated below. The memory is organized as a four mega-word system with 39 bits per word, seven of which are used for error correction code. This system uses 2,496 64K devices organized as 64 rows × 39 columns.

TABLE 7 – HYPOTHETICAL SYSTEM FAILURE RATES

ERROR DESCRIPTION	FAILURE RATE	MTBF
1 soft error in system	1.24×10^{-3} errors/hr.	33.4 days
1 hard error in system	2.5×10^{-4} errors /hr.	166.6 days
2 soft errors in 1 word	1.81×10^{-13} errors/hr.	6.3×10^{8} years
2 hard errors in 1 word	4.74×10^{-10} errors/hr.	241×10^{3} years
1 hard error followed by 1 soft error in 1 word	1.90×10^{-5} errors/hr.	6 years
1 soft error followed by 1 hard error in 1 word	3.8×10^{-6} errors/hr.	30 years

The error probability for the preceding results is given by:

$$P_B = \frac{n!}{r!\,(n-r)\,!} \times p^r \,(1-p)^{(n-r)}$$

where
n = number of bits in the block of interest
r = number of bits in error
p = error probability for a single bit
and given that there is a random error distribution.

The p is derived initially by taking the failure rate in errors/device-hours and dividing it by the number of bits per device to get the error probability for a single bit in errors/bit-hour. For soft errors:

$$p_S = \frac{0.05\%\ \text{errors/device in 1000 hours}}{65{,}536\ \text{bits/device}} = 7.63 \times 10^{-12}\ \text{errors/bit-hour}$$

For hard errors, it has been found that about 25 percent of all hard failures occur in a single cell. Another 25 percent occur in an entire row, while the remaining failures disfunction an entire device. According to this, hard failures are given by:

$$p_H = \frac{0.02\%\ \text{errors}}{\text{device in 1000 hrs.}}\ \frac{25\%\ \text{each bit}}{65{,}536\ \text{bit/device}} + \frac{25\%\ \text{each row or col}}{256\ \text{row or col/device}} + 50\%\ \text{each device} = 1.0 \times 10^{-7}\ \text{errors/device-hr.}$$

Note: This is in errors/device-hour and n and r become number of devices in block of interest and in error, respectively, and p_H is error probability for a single device.

For p of this magnitude, equation (1) reduces to

$$P_B = \frac{n!}{r!\,(n-r)\,!}\ p^r$$

In cases 1 and 2 of the example the block of interest is simply the entire system. In cases 3 and 4, the block of interest is 1 word, and the number of bits is 2. The resulting P_B is then multiplied by the number of words in the system. In case 5 it is assumed that a device has failed, and the block of interest becomes the rest of the words affected by that device failure. Conversely for case 6 it is assumed that a soft error has occurred and the block of interest becomes the devices that contain the rest of the word.

THE ROLE OF SYSTEM DESIGN

The greatest single contributor to system reliability is conservative design. Knowing the environment in which the system is expected to operate dictates many design considerations. Since semiconductor device propagation delays vary with operating temperatures, voltage, etc., care must be given to worst-case design. In many examples, textbook delays do not account for delay in the system as implemented. PC traces and wires are not instantaneous transmission lines nor are they free from noise.

In a design where timing is critical, improperly terminated signals may result in glitches that appear for specific signal sequences only. Poor ventilation may cause operating temperatures to be as high as 30 °C above ambient. Faster cycle times generally mean higher power dissipation. A system operating well at one cycle time may actually slow down as cycle time increases due to the greater propagation delays at higher temperatures.

In some systems the use of sockets may be necessary to facilitate failed device replacement, but many sockets exhibit failure after two or three insertions or repetitive temperature cycling as systems are powered up or down. In other systems poor soldering (either not hot enough for good connection or too hot causing excessive device stress) may be more of a reliability problem.

Systems subject to vibration may have parts that lose good electrical contact and cause intermittent failure. The various electrostatic and RF noise environments also lend themselves to poor system reliability so the designer must understand the problems of shielding.

Typically systems are becoming more memory intense and, therefore, the problems most often reveal themselves in the memory and associated interface circuits. A good board layout of the memory array is essential in good system design to minimize signal noise and provide adequate power line decoupling.

After system assembly, a program of burn-in and stress testing can weed out many of the common problems and provide for maximum system reliability.

APPENDIX A

PROCESS TEST FLOW DIAGRAM

PROCESS		PARTS MAT'LS		FLOW CHART	INSPECTION	FREQUENCY
SILICON MATERIALS PROCESS	PULLERS		○	POLY	CONTAMINATION	EVERY CHARGE
			□	INSPECT	RESISTIVITY	
			○	DOPANT		
			○	GROWN XTAL		
			□	INSPECT	DIMENSIONAL	EVERY CRYSTAL
			○	HEAT TREAT		
			○	CROP		
			□	INSPECT	RESISTIVITY TYPE ETCH PIT OXYGEN	EVERY CRYSTAL
			○	DIAMETER GRIND AND FLAT		
			□	INSPECT	DIAMETER FLAT ORIENTATION APPEARANCE	EVERY CRYSTAL
	SAWING		○	CRYSTAL MOUNT		
			○	ORIENTATION SET-UP		
			□	INSPECT	X-RAY	EVERY CRYSTAL
			○	CRYSTAL SLICING		
			□	THICKNESS CHECK	DIMENSION	100%
			○	ULTRASONIC CLEAN		
	MATERIAL PREPARATION		○	LOT PREP		
			○	EDGE GRIND		
			□	INSPECT	EDGE PROFILE SURFACE CONDITION	100%
			○	ULTRASONIC CLEAN		
			○	HEAT TREAT		
			○	LAP		
			□	INSPECT	DIMENSION	EVERY LOT
			○	ULTRASONIC CLEAN		
			○	STRESS RELIEF		

Legend: ○ Manufacturing
□ Inspection/Log Acceptance
▽ Parts & Materials Inputs

(continued on next page)

PROCESS		PARTS MAT'LS		FLOW CHART	INSPECTION	FREQUENCY
SILICON MATERIAL PROCESS	MATERIAL PREPARATION		○	ETCH		
			□	INSPECT	VISUAL	100%
			□	RESISTIVITY SORT	RESISTIVITY	100%
					DIMENSIONAL	
			□	LOT ACCEPTANCE	DIMENSIONAL SURFACE QUALITY EDGE QUALITY, RESISTIVITY	EVERY LOT
			○	EPITAXIAL FORMATION	QUALITY	100%
FRONT END PROCESS	PREPARATION		○	SILICON WAFERS (EPI)	DIMENSIONAL RESISTIVITY	EVERY LOT
			□	INSPECT	TAPER, BOW	
			○	CLEANUP A		
			○	SPIN SWAB		
	MOAT FORMATION		○	OXIDATION		
			□	MONITOR PLOT	AUTO THICKNESS	EVERY LOT
			○	INITIAL NITRIDE		
			□	PILOT	AUTOMATIC ELECTRICAL	EVERY LOT
		MASK	▽ ○	SPIN SWAB		
			□	MASK INSPECT	AUTOMATIC VISUAL	EVERY 5 LOTS
			○	INVERSE MOAT		
			○	O. R.		
			□	INSPECT	VISUAL	100% SLICES
			○	PLASMA ETCH		
			□	MEASURE	SEMI-AUTOMATIC	EVERY LOT
			□	P.C. INSPECT	VISUAL	EVERY LOT
			○	CHANNEL STOP IMPLANT		
			○	CLEANUP B		

Legend: ○ Manufacturing
□ Inspection/Lot Acceptance
▽ Parts & Materials Input

O.R. = Oxide Removal
P.C. = Process Control

(continued on next page)

PROCESS		PARTS MAT'LS		FLOW CHART	INSPECTION	FREQUENCY
FRONT END PROCESS	MOAT FORMATION		○	N_2 ANNEAL		
			□	PILOT	AUTO THICKNESS	EVERY LOT
			○	THICK OXIDATION		
			□	PILOT	AUTO THICKNESS	EVERY LOT
			○ □	MOAT ETCH INSPECT	VISUAL	EVERY LOT
	FIRST GATE FORMATION		○	CLEANUP C		
			○	GATE OXIDATION		
			□	PILOT	AUTO THICKNESS, AUTO ELECTRICAL	EVERY LOT
			□	P.C. INSPECT	VISUAL	EVERY LOT
			○	V_{tx} ADJUST IMPLANT		
	FIRST POLY FORMATION		○	CLEANUP D		
			○	POLYSILICON DEPOSITION		
			□	INSPECT	VISUAL	EVERY LOT
			○	SPIN SWAB		
			○	PHOSPHOROUS DEPOSITION		
			□	MEASURE	AUTO ELECTRICAL	EVERY LOT
		MASK	▽ ○	DEGLAZE		
			□	MASK INSPECT	AUTO VISUAL	EVERY 5 LOTS
			○	POLY I PATTERN		
			□	INSPECT	VISUAL	100% SLICES
			○	POLY I ETCH		
			□	MEASURE	SEMI-AUTO	EVERY LOT
			□	P. C. INSPECT	VISUAL	EVERY LOT
			○	CLEANUP E		

Legend: ○ Manufacturing
□ Inspection/Lot Acceptance
▽ Parts & Materials Input

P.C. = Process Control

(continued on next page)

PROCESS		PARTS MAT'LS		FLOW CHART	INSPECTION	FREQUENCY
FRONT END PROCESS	SECOND POLY FORMATION		○	INTERLEVEL GATE OXIDATION		
			○	V_{tx} ADJUST IMPLANT	AUTO THICKNESS	EVERY LOT
			□	PILOT	AUTO ELECTRICAL	EVERY LOT
		MASK	▽ ○	POLYSILICON DEPOSITION		
			□	INSPECT	VISUAL	EVERY LOT
			○	POLY II PATTERN		
			□	INSPECT	VISUAL	EVERY LOT
			○	POLY II ETCH		
			□	MEASURE	SEMI-AUTO VISUAL	EVERY LOT
			□	P.C. INSPECT	VISUAL	EVERY LOT
	SOURCE DRAIN FORMATION		○	CLEANUP F		
			○	CLEANUP G		
			○	BAKE OUT		
			○	ARSENIC IMPLANT		
			□	PILOT	AUTO ELECTRICAL	EVERY LOT
			○	REOXIDATION		
	METALLIZATION PREPARATION, FORMATION		□	PILOT	AUTO THICKNESS	EVERY LOT
			○	MULTILEVEL DEPOSITION		
		MASK	▽ ○	DENSIFICATION		
			□	PILOT	AUTO ELECTRICAL	EVERY LOT
			○	2nd CONTACT OX-IDE REMOVAL		
			□	INSPECT	VISUAL	100% SLICES
			□	P. C. INSPECT	VISUAL	EVERY LOT
			○	CLEANUP H		
			○	REFLOW ARGON		

Legend: ○ Manufacturing
□ Inspection/Lot Acceptance
▽ Parts & Materials Input

P.C. = Process Control

(continued on next page)

PROCESS		PARTS MAT'LS		FLOW CHART	INSPECTION	FREQUENCY
FRONT END PROCESS	METALLIZATION PREPARATION FORMATION		□	PILOT	AUTO ELECTRICAL	EVERY LOT
			○	POST ARGON REFLOW ANNEAL		
		MASK	▽ ○	PREMETAL CLEANUP		
			□ ○	METAL SPUTTER		100% SLICES
			○	METAL PATTERN		
			□	INSPECT	VISUAL	100% SLICES
			○	METAL ETCH		
			□	INSPECT	VISUAL	100% SLICES
	OVERCOAT		○	H_2 BAKE		
			□	TEST PROBE	FUNCTIONAL	EVERY LOT
		MASK	▽ ○	PLASMA NITRIDE P.O.		
			□ ○	P.O. PATTERN		
			□	INSPECT	VISUAL	100% SLICES
			○	P.O. PLASMA ETCH + ASH		
			□	P.C. INSPECT	VISUAL	EVERY LOT
	TEST		○	BACKGRIND		
			○	BACKSIDE GOLD EVAPORATION		
			○	MULTIPROBE	MECHANICAL	100% SLICES
			□	FINAL P.C. INSPECT	VISUAL/PAPERWORK	EVERY LOT

Legend:
- ○ Manufacturing
- □ Inspection Lot Acceptance
- ▽ Parts & Materials Input

P.C. = Process Control
P.O. = Protective Overcoat

APPENDIX B

ASSEMBLY TEST FLOW DIAGRAM

PROCESS		PARTS MAT'LS		FLOW CHART	INSPECTION	FREQUENCY
ASSEMBLY PROCESSING	ASSEMBLY PROCESS		○	SAWING, BREAKING		
			□	INSPECT	VISUAL	EVERY LOT
		LEAD-FRAME POLY-MIDE	▽ □	LEADFRAME CONTROL POLYMIDE	DIMENSION VISUAL BONDABILITY BAKE ANALYSIS	EVERY LOT
			○	DIE MOUNT		
			□	INSPECT	VISUAL	EVERY LOT
		GOLD WIRE	▽ □	GOLD WIRE CONTROL	VISUAL PULL STRENGTH ELONGATION CURLING DIAMETER ANALYSIS	
		POLY-MIDE 2 SHIELD	○	WIRE BONDING		
	FINISHING PROCESS		▽ □ □	INSPECT	BOND STRENGTH VISUAL	EVERY LOT EVERY LOT
			○	ALPHA SHIELD APPLICATION	WEIGHT CONTROL	EVERY SHIPMENT
		MOLDING COM-POUND	▽ □ ○	MOLDING COMPOUND CONTROL VISUAL	FLOW LENGTH FILLER CONTENT	EVERY LOT
			○	CURING	GLASS TRANSITION	
			□	INSPECT MOLDING	VISUAL	EVERY LOT
			□	INSPECT	VISUAL	EVERY LOT
			○	CURING		
			○	LEAD PLATING		
			□	INSPECT	PLATING THICKNESS SOLDERABILITY	EACH DAY EVERY LOT
			○	SHEAR/FORM		
			□	INSPECT	VISUAL DIMENSION	EVERY LOT

Legend: ○ Manufacturing
□ Inspection/Lot Acceptance
▽ Parts & Materials Input

(continued on next page)

PROCESS		PARTS MAT'LS		FLOW CHART	INSPECTION	FREQUENCY
TEST FLOW	TESTING		□	ELECTRICAL	ELECTRICAL CHARACTERISTICS	100%
			▽ ○	SYMBOLIZATION		
	INSPECTION		□	QRA LOT ACCEPTANCE	ELECTRICAL CHARACTERISTICS VISUAL MECHANICAL	EVERY LOT
			○	RECEIVE LOTS FROM OFFSHORE		
	ELECTRICAL TESTING		□	QRA MONITOR VISUAL & MECHANICAL	25 °C HI/LO TEMP	SKIP LOT MONITOR
			□	RELIABILITY TEST	85 °C/85% RH 1000 HR. LIFE TEST TEMP CYCLE PRESSURE COOKER	MONTHLY
	SHIPPING		○	PACKING	FINAL SHIPMENT QUANTITY SHIPPING DOCUMENTATION	100%
			⇨	SHIPPING QRA	DOCUMENTATION QUANTITY, VISUAL, MECHANICAL LOT ACCEPTANCE	

Legend: ○ Manufacturing
□ Inspection/Lot Acceptance
▽ Parts & Materials Input

APPENDIX C

TMS 4164 FINAL TEST

To ensure the highest in quality and performance, each MOS memory device manufactured by Texas Instruments MOS Memory Division is thoroughly tested before shipment. Testing is accomplished during assembly by process engineering (indicated on the manufacturing flow charts in the previous Appendix). Testing is also done after assembly by product engineering (final test), and after final test by quality and reliability assurance engineering (QRA). Every device is tested during the first two stages after which they are received by QRA for random screening for reliability. Outlines of the final test procedure and QRA screening process by family type are included in this Appendix.

TABLE C-1 – 64K DYNAMIC RAM – FINAL ASSEMBLY TEST FLOW

Pre-Burn-In Screening	Verifies electrical and timing parameters at worst-case limits. V_{DD} = 4.35 V, 5.65 V Temperature = 25 °C Guardband testing for 0 °C operation
Burn-In	All product is dynamically burned in to the following conditions: V_{DD} = 7 V, Temperature = 125 °C 1 microsecond cycle time, 50% duty cycle
Post Burn-In Screening	Extensive parametric and functionality testing at worst-case supply voltages. Temperature = 86 °C for ceramic, 90 °C for plastic.
Quality Acceptance	Quality and Reliability Assurance Group
Lot Acceptance Testing	Visual and mechanical inspection Parametric and functionality test at worst-case supply voltages, low and high temperatures

TABLE C-2 — TMS 4164 FINAL TEST

TEST NAME	TEST DESCRIPTION
PARAMETRIC SECTION	
Continuity	Check for lead-to-bond pad integrity and high substrate resistance. Force 80 microamperes on pin under test (PUT) and measure voltage. This is done on all used pins.
Input Leakage	Bias V_{DD} to 5.5 volts. Open the output. The PUT is biased to 5.5 volts with all others at 0 volts. Read the current. The PUT is then biased to 0 volts with all others at 5.5 volts. Read the current.
Output Leakage	Bias V_{DD} to 5.5 volts. Bias all input and clock pins to V_{IH}. The output current I_O is measured with PUT biased to V_{OH} and V_{OL}.
I_{DD} Ave. Operating	Measure the average supply current I_{DD} under dynamic conditions. V_{DD} = 5.5 volts, t_C = 350 nanoseconds, output open.
I_{DD} RAS Only (Refresh)	Same with CAS = V_{IH} continuously.
I_{DD} Standby	With V_{DD} = 5.5 volts, cycle device under test (DUT) once and wait 50 ms and read I_{DD}. The input and clock pins will be at V_{IH}.

TABLE C-2 — TMS 4164 FINAL TEST (Continued)

PATTERN NO.	TEST NAME	TEST DESCRIPTION
		FUNCTIONAL SECTION
1.	Address Select	Using row fast addressing, the array is written with an all "0" pattern. For each address starting at 0000_H, the following is performed: Read the "0"; write a "1"; read the "1"; increment the address sequentially. Starting at 0000_H again at each location, read the "1", write a "0", read the "0", increment sequentially through the array. This algorithm checks the address decode, read and write operations. Repeat the pattern decrementing the address from $FFFF_H$.
2.	Checkerboard	Using row fast addressing, write an alternating data pattern into the array of "1"s and "0"s. The result is a checkerboard pattern. Read the pattern and check for valid output. The pattern register is complemented, an inverse checkerboard pattern is written and read back sequentially.
3.	Walking "1" & "0"	Using row fast addressing, write the array with "0"s. In the column fast direction, read the "0", write a "1", read the "1", rewrite a "0" at each location. When the last address is reached ($FFFF_H$), complement the data and repeat. Under column fast mode, refresh interrupt must be performed every 4 milliseconds. This routine checks proper sense and direction and also compares data that's surrounded by its complement.
4.	Sliding Diagonal	A background of "1"s is written sequentially. A diagonal stripe develops by writing a "1" at address 0000_H, complementing the address and rewriting a "1". The address is incremented along the diagonal and the procedure continues until the stripe is completed. The data is read back from the diagonal in the same fashion. The diagonal is then shifted one column at a time until each diagonal stripe is completed. The routine is repeated with complement data.
5.	Horizontal and Vertical Stripes	Write pattern of alternating data in each row that will result in horizontal stripes of "1"s and "0"s. Read the data in the same fashion. Write a pattern of "1"s and "0"s in each column to form vertical stripes. Read back the data. The routine is repeated with complement data.
6.	Gray Code	This is a disturb refresh test that uses modified Gray code to determine the x address of the disturbs. Write the test row with "0"s. Write "1"s in 8 distinct rows, generated by the Gray code with the test row as a base. Do this for the 4 ms refresh period. Read back the test row to verify data retention capability. Do this for each row and repeat with complement data. Using the modified Gray code ensures that the adjacent row and at least one row on the opposite side of the sense amplifiers are disturbed.
7.	Burst Refresh	This is the same as the checkerboard with the exception that there is a 4 ms wait period before reading back the data.

TABLE C-2 — TMS 4164 FINAL TEST (Concluded)

PATTERN NO.	TEST NAME	TEST DESCRIPTION
	FUNCTIONAL SECTION	
8.	Voltage Slew	Same as checkerboard except that data is read at a different V_{DD} value than that at which it is written.
9.	Long Cycle Test	This is the same as checkerboard with a cycle time of 10.2 microseconds. The DUT is checked with a $\overline{RAS}$ pulse width of 10 microseconds. The write is done late in the cycle. The comparison for valid data is also done late in the cycle to verify data out integrity after 10 microseconds.
10.	Page Mode	Test verifies page mode operation by checking the DUT performance under constant row address with varying column addresses. The column address is incremented sequentially. Each row is paged, but the maximum number of columns that can be done in one $\overline{RAS}$ cycle is a function of $t_{c(P)}$ and $t_{w(RL)}$ maximum.

All patterns are developed on 100 percent of the array with various voltage and timing conditions. Table C-3 describes these conditions.

TABLE C-3 – CONDITIONS USED FOR TMS 4164 PATTERNS*

TEST	PATTERN NUMBER							
	1	2	3	4	5	6	7	8
V_{DD} MIN	X	X	X	X	X	X	X	
V_{DD} MAX	X	X	X	X	X	X		
V_{IH} MIN	X	X	X	X	X	X	X	X
V_{IH} MAX		X	X		X			
V_{IL} MIN			X		X			
V_{IL} MAX	X	X	X	X	X	X	X	X
t_c MIN	X		X	X	X	X	X	X
T_A MAX	X		X	X	X	X	X	X
$t_{w(RL)}$ MIN	X		X	X	X	X	X	X
$t_{w(RL)}$ MAX	X			X		X	X	X
$t_{w(RH)}$ MIN		X	X		X			
$t_{w(W)}$ MIN	X		X	X	X	X	X	X
$t_{su(CA)}$ (RA) (D)	X		X	X	X	X	X	X
$t_{h(RLCA)}$	X		X	X	X	X	X	X
$t_{h(CLCA)}$	X		X	X		X		X
$t_{h(RA)}$		X	X	X		X		
$t_{h(RLW)}$ (CLD)	X		X	X	X	X	X	X
$t_{h(CLW)}$ (CLD)	X		X	X	X	X		X
$t_{su(WCH)}$		X	X	X		X		
$t_{su(WRH)}$	X		X	X		X		X
t_{rf} MAX			X	X	X	X	X	

* Any pattern that has two mutually exclusive conditions tested, such as V_{DD} MIN and MAX, implies the pattern is tested more than once.

Characterization testing is also performed on 10 random part samples. Table C-4 shows the results of such testing.

TABLE C-4 – CHARACTERIZATION DATA FOR TMS 4164-15
(Timing Requirements in Nanoseconds)

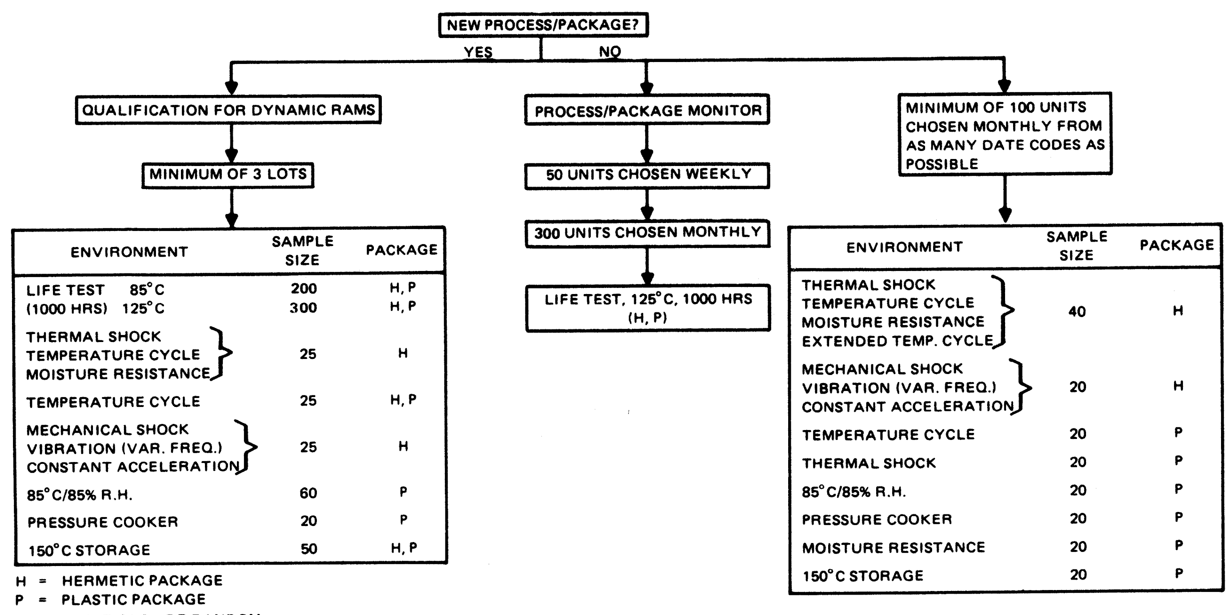
PARAMETERS	83°C*	0°C*	SPECIFIED VALUE
$t_{w(CH)}$	11		50
$t_{w(CL)}$	62		100
$t_{w(RH)}$	52	42	100
$t_{w(W)}$	12		45
$t_{su(WCH)}$	25	18	60
$t_{su(WRH)}$	44		60
$t_{h(RA)}$	6		20
$t_{h(RLCA)}$	70		95
$t_{h(CLCA)}$	16		45
t_{RLCH}	107		150
$t_{h(CLD)}$	30		60
$t_{h(RLD)}$	86		125
$t_{h(CLW)}$	34		60
$t_{h(RLW)}$	89		125
$t_{a(R)}$	126		150
t_{RLCL}	0-65		20-50
t_{CLWL}	23		40
$t_{a(C)}$	69		100
$t_{su(CA)}$		−12	−5
$t_{su(RA)}$		−7	0
$t_{su(D)}$		−9	0
$t_{w(RL)}$	128		170

* Average measured value.

As demonstrated by this characterization data, the TMS 4164-15's tested operate well within specification margins under worst-case conditions.

APPENDIX D

QUALITY AND RELIABILITY



ENVIRONMENT	SAMPLE SIZE	PACKAGE
LIFE TEST 85°C (1000 HRS)	200	H, P
LIFE TEST 125°C (1000 HRS)	300	H, P
THERMAL SHOCK TEMPERATURE CYCLE MOISTURE RESISTANCE	25	H
TEMPERATURE CYCLE	25	H, P
MECHANICAL SHOCK VIBRATION (VAR. FREQ.) CONSTANT ACCELERATION	25	H
85°C/85% R.H.	60	P
PRESSURE COOKER	20	P
150°C STORAGE	50	H, P

H = HERMETIC PACKAGE
P = PLASTIC PACKAGE
ALL SELECTIONS ARE RANDOM
LIFE TEST UNITS ELECTRICALLY TESTED; PACKAGE ENVIRONMENTS FOLLOWED BY ELECTRICAL AND HERMETICITY (H ONLY) TESTS

ENVIRONMENT	SAMPLE SIZE	PACKAGE
THERMAL SHOCK TEMPERATURE CYCLE MOISTURE RESISTANCE EXTENDED TEMP. CYCLE	40	H
MECHANICAL SHOCK VIBRATION (VAR. FREQ.) CONSTANT ACCELERATION	20	H
TEMPERATURE CYCLE	20	P
THERMAL SHOCK	20	P
85°C/85% R.H.	20	P
PRESSURE COOKER	20	P
MOISTURE RESISTANCE	20	P
150°C STORAGE	20	P

FIGURE D-1 – 64K DYNAMIC RAM QUALITY AND RELIABILITY FLOW

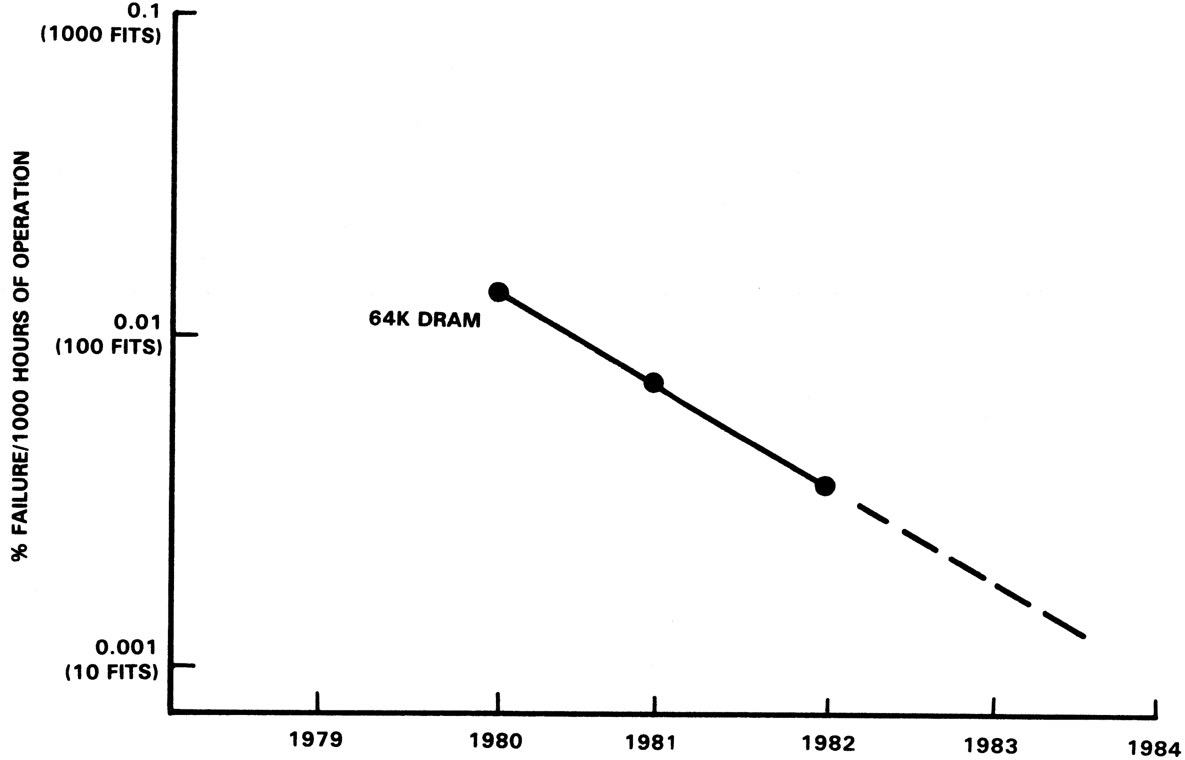


FIGURE D-2 – DRAM RELIABILITY FORECAST

APPENDIX E

ORGANIZATION CHART

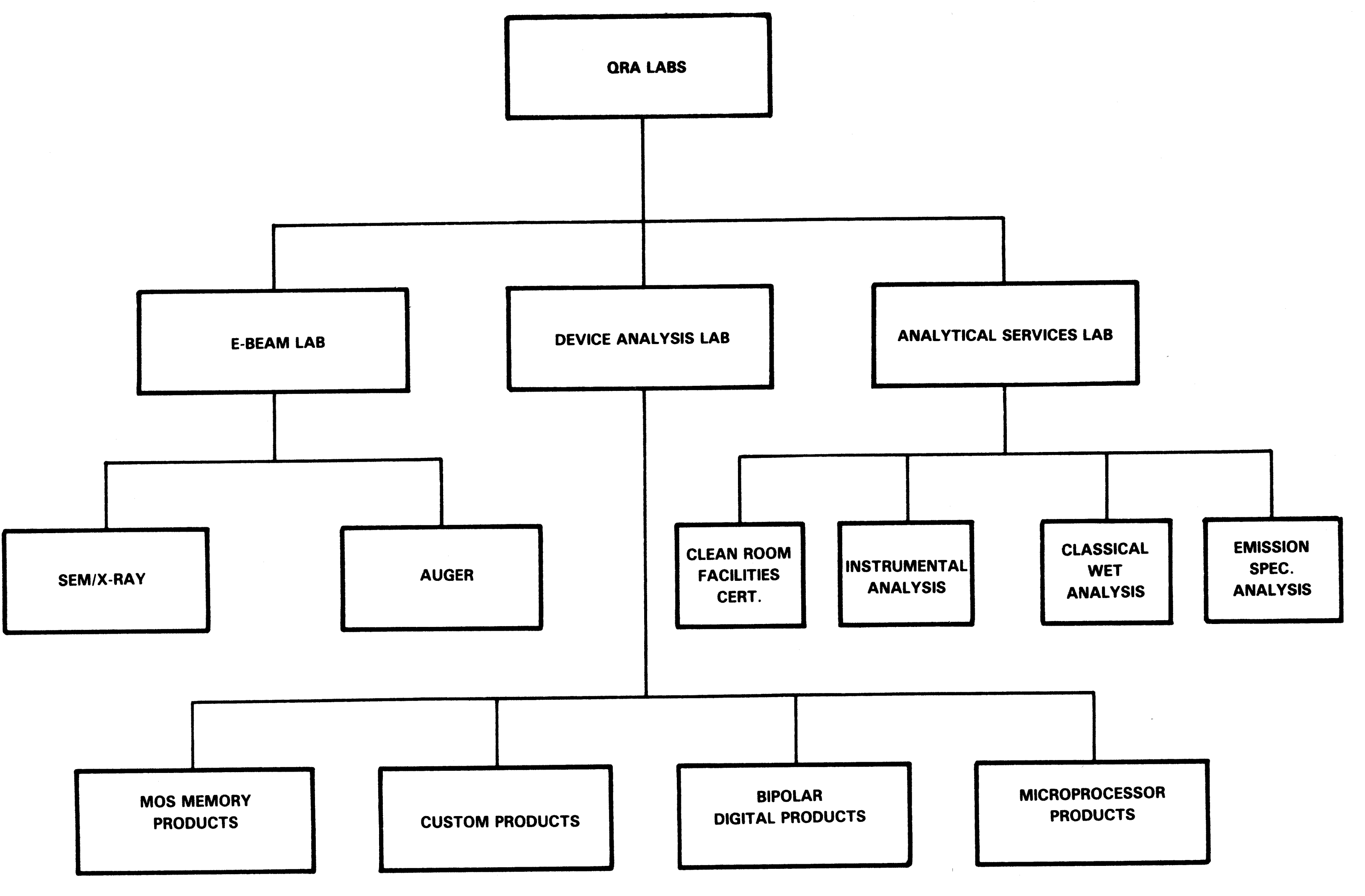


FIGURE E-1 – HOUSTON QRA LABORATORIES ORGANIZATION CHART

APPENDIX F

FAILURE ANALYSIS

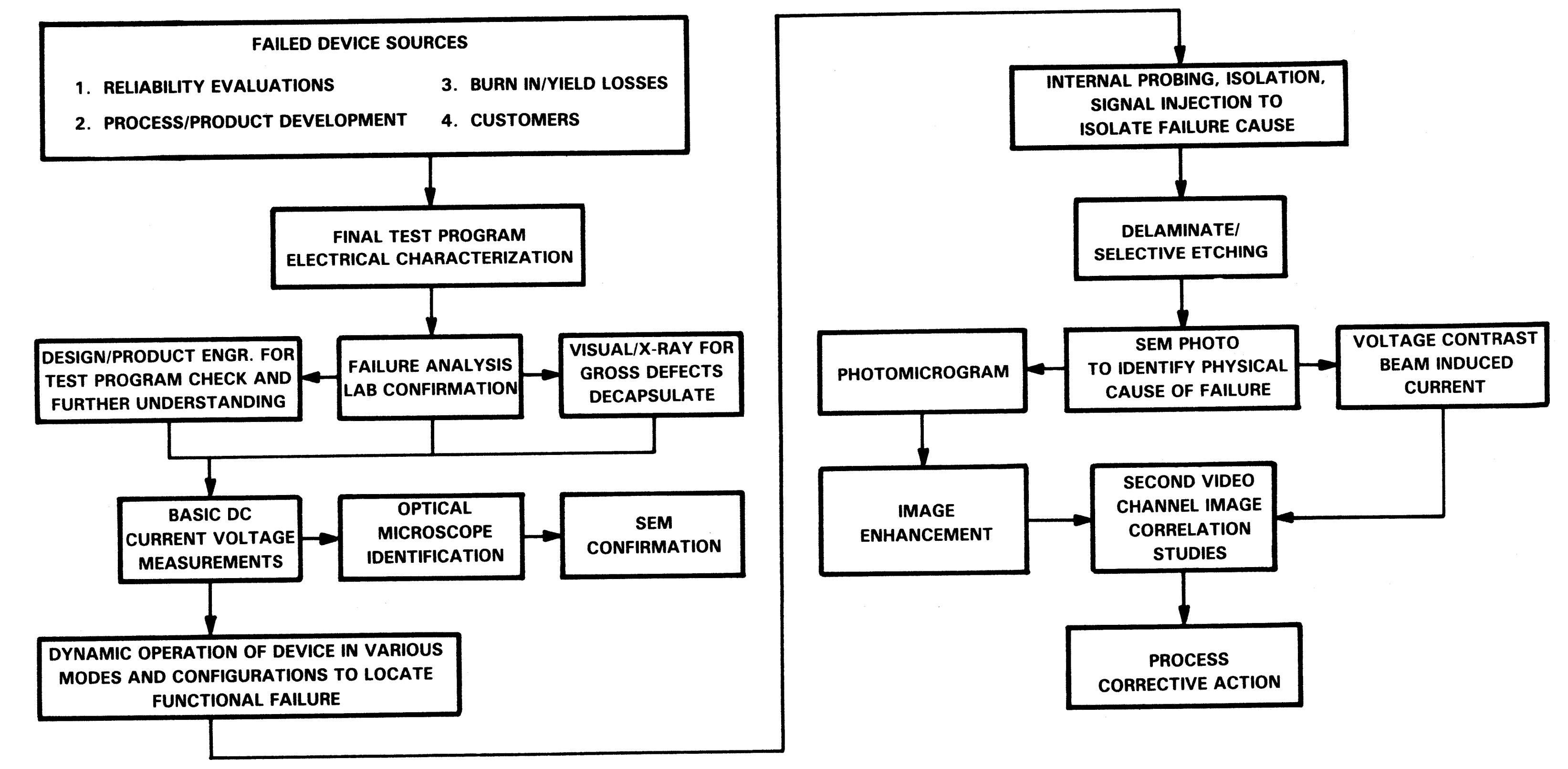


FIGURE F-1 – FAILURE ANALYSIS FLOW

APPENDIX G

MANUFACTURING SUPPORT

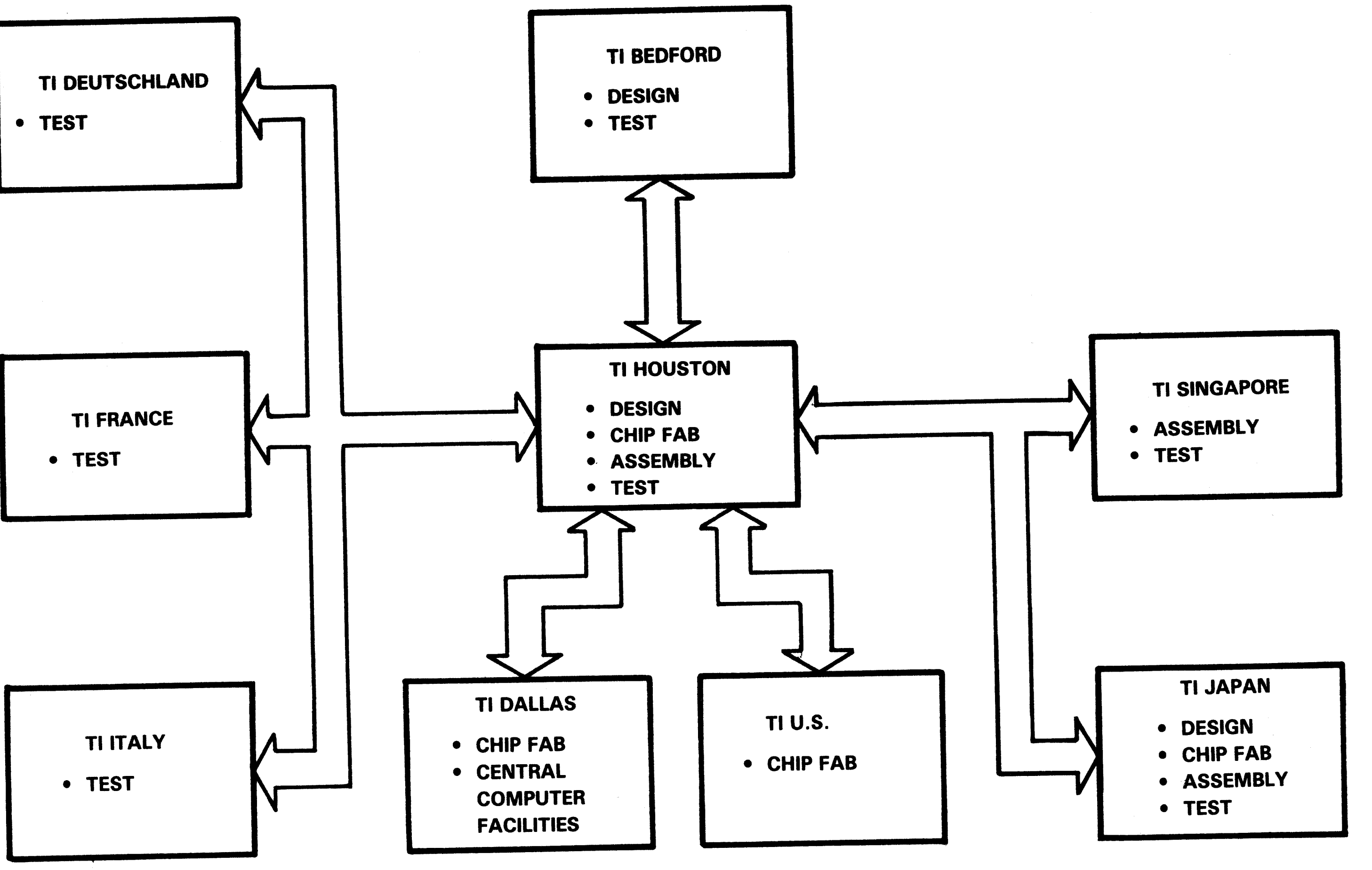


FIGURE G-1 — MOS DYNAMIC RAM WORLDWIDE MANUFACTURING SUPPORT

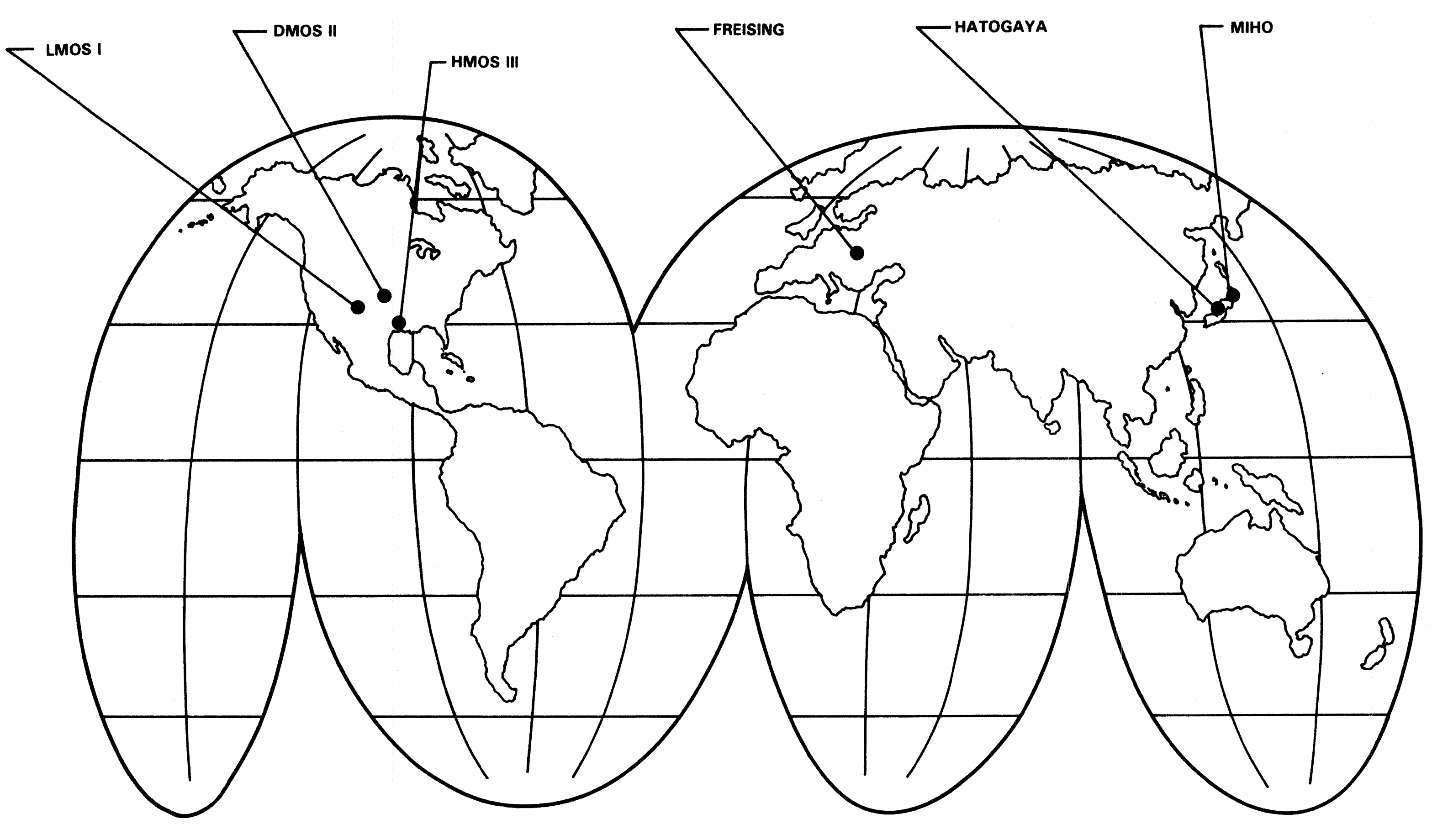


FIGURE G-2 – MOS FRONT END FACILITIES

APPENDIX H

SYSTEM TEST FIXTURE

INTRODUCTION

The system test fixture (STF) is a memory testing device capable of universal testing of dynamic RAMs under various system operating conditions. Tests can be performed using up to seven different programmable waveform generators that are controlled by a microprogram control store unit. The waveforms are assigned to $\overline{RAS}$, $\overline{CAS}$, $\overline{W}$, Data In Strobe, Data Out Strobe, and Address Multiplex to control and test existing multiplexed address dynamic memories. These signals can provide for read, write, read-write, and refresh cycles. Refresh can be programmed through software and/or provided for in hardware in a synchronous manner. Internal registers include a 24-bit data generator, a 20-bit address generator, a 20-bit address pointer, and a 24-bit general purpose counter. These registers provide the information to run various types of addressing and data pattern tests. In addition, the DRAM voltage may be programmed.

A block diagram of the STF is shown in Figure H-1. Each of the blocks and its overall function within the system is explained later.

CYCLE GENERATOR

The Cycle Generator is a programmable cycle time oscillator that produces pulses of various widths to drive the pulse generators. The cycle time can be programmed from 200 nanoseconds to 1 microsecond in 5-nanosecond increments. This generator also produces the clocks that are needed for the Control Store unit of the STF. The cycle time is determined by the number of clock cycles and delay elements selected for that cycle. A 20-megahertz clock drives the shift register. One of the outputs of the shift register is selected by an 8:1 multiplexer. A finer delay of 0 – 50 nanoseconds is then selected by the program inputs to the finer delay unit. At the end of this delay period an identical unit to the one just described (programmed with identical inputs) will provide the next cycle. Each half of the pulse generator outputs every other cycle. The output for each half is a series of pulses starting at 50-nanosecond intervals. These pulses then drive the inputs to the pulse generators.

PULSE GENERATORS

The Pulse Generators take the outputs of the cycle generators and make a single output wave reflecting the program inputs. The outputs of the pulse generators have a cycle time equal to the cycle generators cycle time, but have a pulse width of from 0 to the cycle time in 5-nanosecond increments. This is done using a technique similar to the cycle generator shown in Figure H-2.

The cycle generators and pulse generators time the signals required for the dynamic RAMs. The cycle generator also outputs the 3-phase clocks needed for the Control Store unit. Under control of this unit, the programmed sequence of read, write, refresh, and read/write cycles gates the signals to the RAMs.

CONTROL STORE

Within the programmable Control Store unit, the decisions are made to perform either a read, write, read/write, or a refresh instruction. The Control Store unit also selects the data pattern to be written, the address sequence to be followed, and the sequence of tests to be run. This is done with a 32-bit Control Store word as shown in Figure H-3.

The Control Store program is stored in a fast bipolar memory. Instructions are fetched and performed in a pipeline fashion to allow instruction times as fast as 200 nanoseconds. An instruction fetch/execute is shown in Figure H-4. The sequence is clocked so that the Control Store fetches the next data word while it is performing the current word task.

The earliest timing signals ($\overline{RAS}$ or ROW address multiplex in the case of dynamic memory) cannot occur before the falling edge of phase 1 to allow the data and address registers to reach their proper value. The selected branch flag, the branch offset, and the current instruction determine the Control Store address. The new Control Store data word is selected in time for decisions on incrementing any of the data registers on the next rising edge of phase 1.

GENERAL PURPOSE COUNTER

The General Purpose Counter is a 24-bit presettable counter. It can be used as a timing counter (count number of loops) and branch when the count equals zero. Any of the six digits can be preset to any value, or all digits can be stored. When instructed by the Control Store word, the counter will decrement.

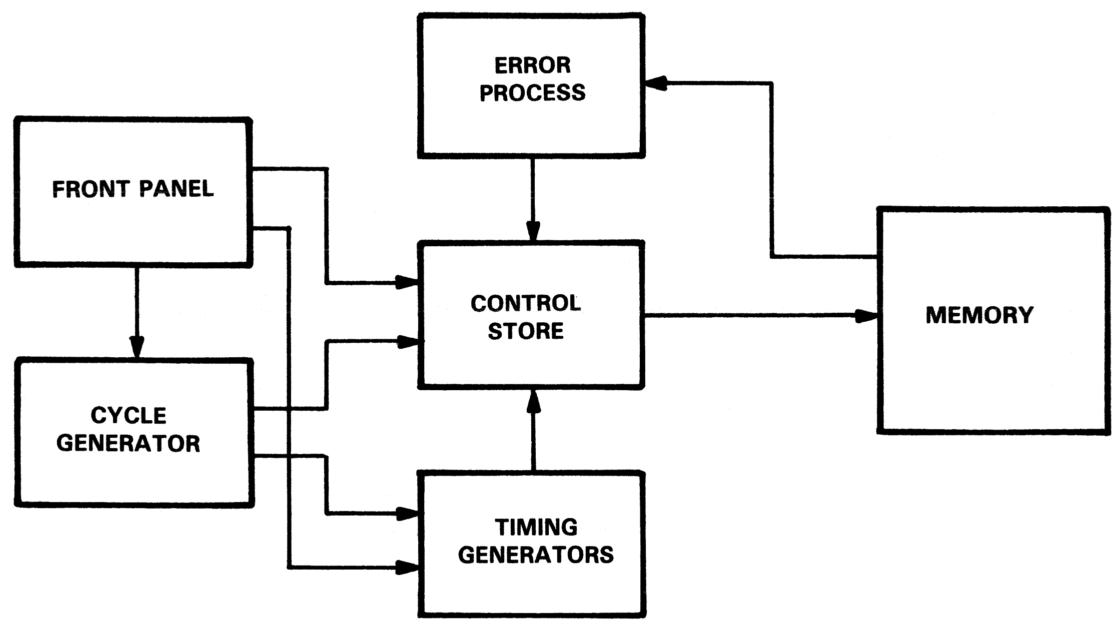


FIGURE H-1 – SYSTEM TEST FIXTURE

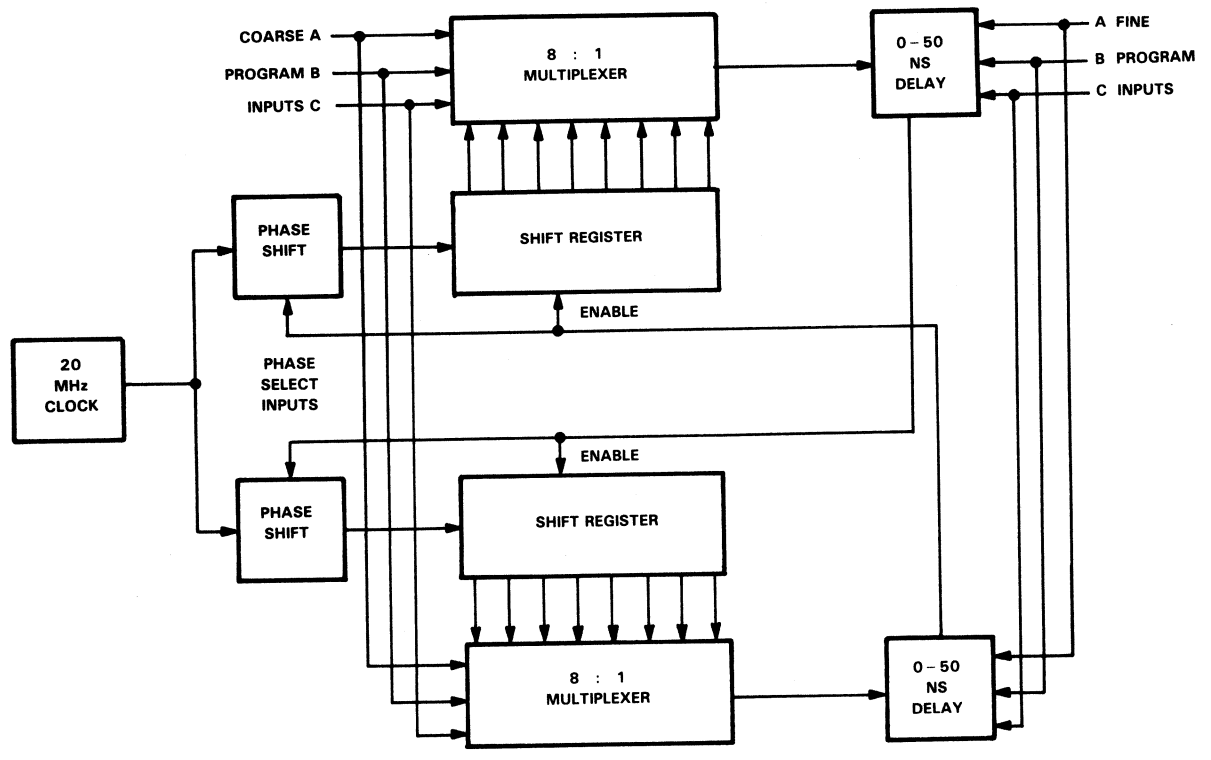


FIGURE H-2 – CYCLE GENERATOR

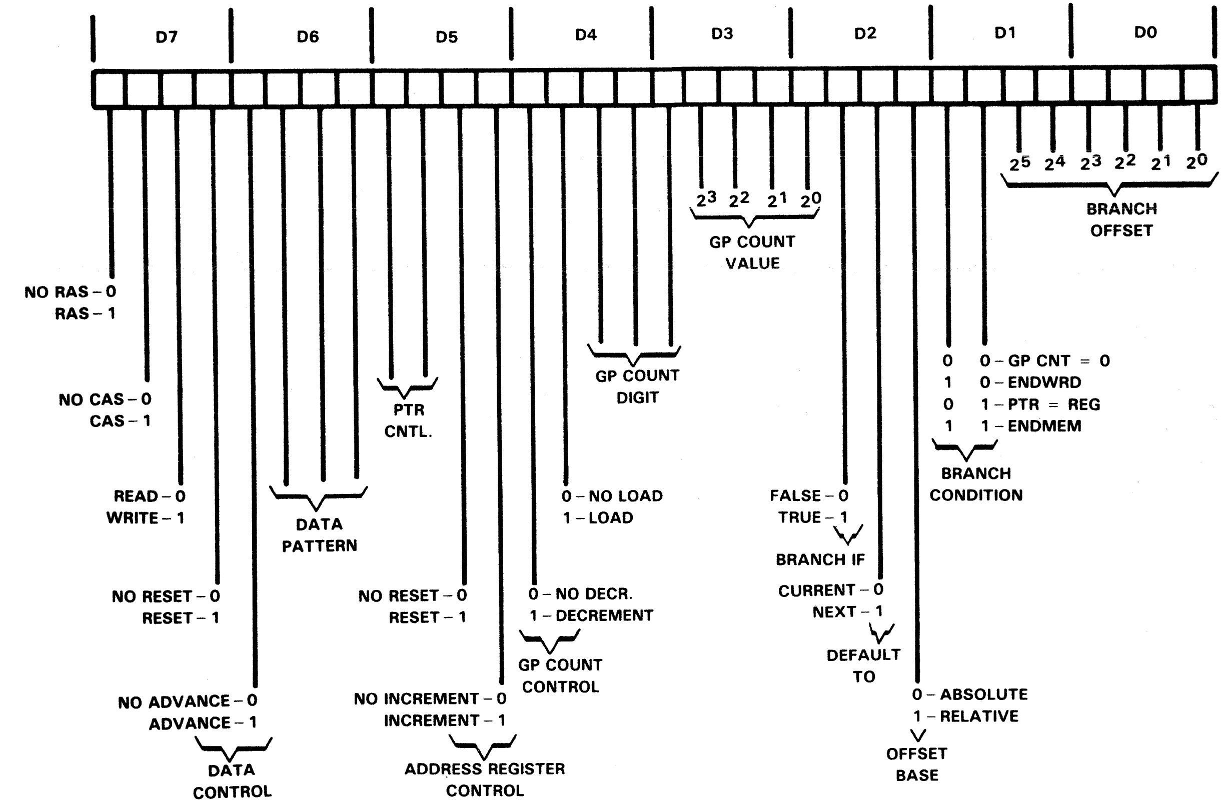


FIGURE H-3 – CONTROL STORE WORD

ADDRESS REGISTER

This is a 20-bit register that contains the address of the memory under test. This address can be reset or incremented as controlled by the Control Store instruction. Branches are possible on end of the memory in which the ending location is programmed via DIP switches on the Control Store board. The address significance can also be programmed to test different pattern sequences. The pattern is programmed with jumpers between source bits and destination lines on the Control Store board.

The address pointer allows another means for keeping track of a particular place in memory. This ''pointer'' can also be reset or incremented in the same way as the address register. The address pointer is compared to the address register and the result is reflected in the ADD = PTR Flag.

DATA GENERATOR

The Data Generator contains the data to be presented to the memory under test. The memory patterns can be classified into two groups: constant patterns and changing patterns. The constant patterns include data fields of all ''1''s, all ''0''s, ''AA''s, and ''SS''s. The changing patterns include walking ''1''s, walking ''0''s, marching ''1''s, and marching ''0''s. The four changing patterns are illustrated in Table H-1. Each of the changing patterns requires an increment instruction from the Control Store word to change the pattern to the next state.

The flag ENDWRD refers to the last state of a changing data pattern. After the last state of a pattern is reached, the Data Generator must be reset before the next pattern is started.

Each of the fields of the Control Store word is individually programmmed to complete the entire Control Store word. This is most easily done with the individual fields separated as shown in Figure H-5.

ERROR PROCESS BOARD

The final block of the STF is the Error Process board. This circuitry interrogates the memory under test. It receives data read from memory and compares it to the data from the data generator. If the data is different anytime during the window, determined by the Data Out Strobe, a flip-flop is set and the error process begins. The Control Store unit will fetch the next instruction from the preprogrammed error address (DIP) switches. The error process routine should then rewrite the location that was in error, reread this location to be sure the error does not persist, then return to the normal program. The error count is incremented when the error is rewritten.

TABLE H-1 – CHANGING PATTERNS

WALK 1	WALK 0	MARCH 1	MARCH 0
0000	1111	0000	1111
1000	0111	1000	0111
0100	1011	1100	0011
0010	1101	1110	0001
0001	1110	1111	0000
0000	1111	0000	1111

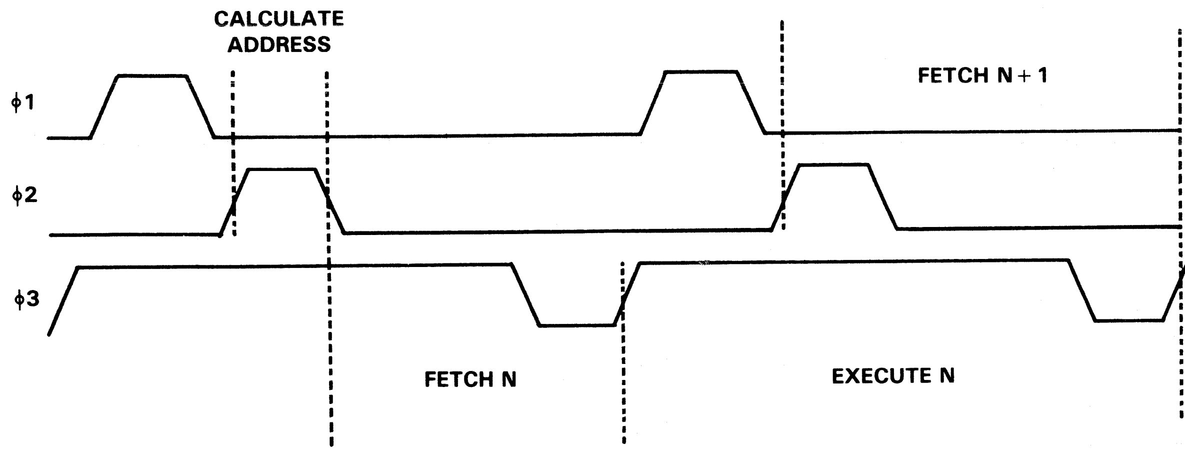


FIGURE H-4 – TIMING DIAGRAM FOR FETCH/EXECUTE INSTRUCTION

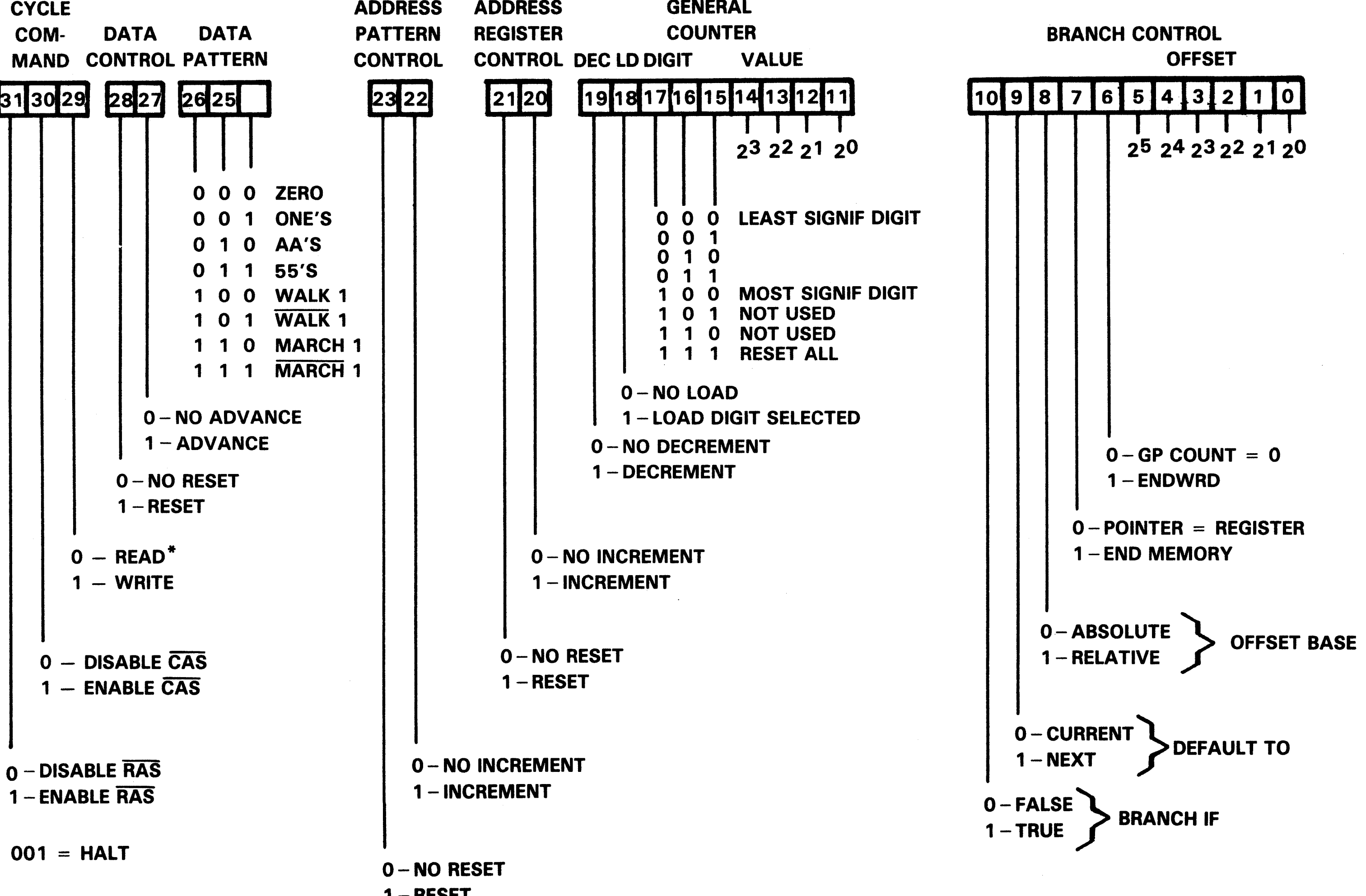


FIGURE H-5 – INDIVIDUAL FIELDS

APPENDIX I

PORTABLE ALPHA TESTER

CIRCUIT DESCRIPTION

The test fixture for the TMS 4164 consists of five major sections: the cycle time control, timing signal generation, address generation and multiplexing, error detection, and display/counter. A 20-megahertz, single-chip oscillator and inverter provide the square wave input signal. Cycle times are variable from 500 nanoseconds to 80 microseconds.

U12, a 74ALS393 dual binary counter, provides cycle times from 400 nanoseconds to 12.8 microseconds by dividing the 20-megahertz input using six of the eight divide-by-2 outputs. $1Q_A$ and $1Q_B$ are not used. U10, a 74LS390, is wired as a divide-by-100 circuit to provide a 5-microsecond output. This signal is fed into a 74S163 binary counter that gives the 10 through 80 microsecond speeds. All counter outputs connect to an 11-position rotary switch, S1.

The wiper of switch S1 is connected to U13, a 74S175 quad D flip-flop, which is connected as a four-bit shift register whose output signals are decoded and latched to provide the timing signals for the TMS 4164.

Addresses for the TMS 4164 are generated by two 74LS393, U1 and U2, from the CAS signal. The inputs for DRAM, MA0-MA7, are multiplexed from the 16 address lines by U3 and U4. A7 is used to write "true ones" or "true zeroes" to the array. Flip-flop U8b controls the $\overline{W}$ line. The test fixture writes to all memory locations and then reads out and compares the input and output data by using XOR gate U5b and flip-flop U8a. The error strobe is timed and controlled by 74LS02 NOR gates U6a and U6b.

The error strobe drives the counter/display board composed of five TIL 306s. The Reset switch is connected to the clear pins of the counters.

OPERATING INSTRUCTIONS

Follow the steps as outlined below:

1. Turn on power
2. Select speed of cycle
3. Install delidded TMS 4164 in textool socket, pin 1 at top, and position alpha source on TMS 4164. Center source over chip for accurate readings.
4. Select true/complement data
5. Reset and time from the release of the Reset switch

FIGURE I-1 – PORTABLE ALPHA TESTER SCHEMATIC

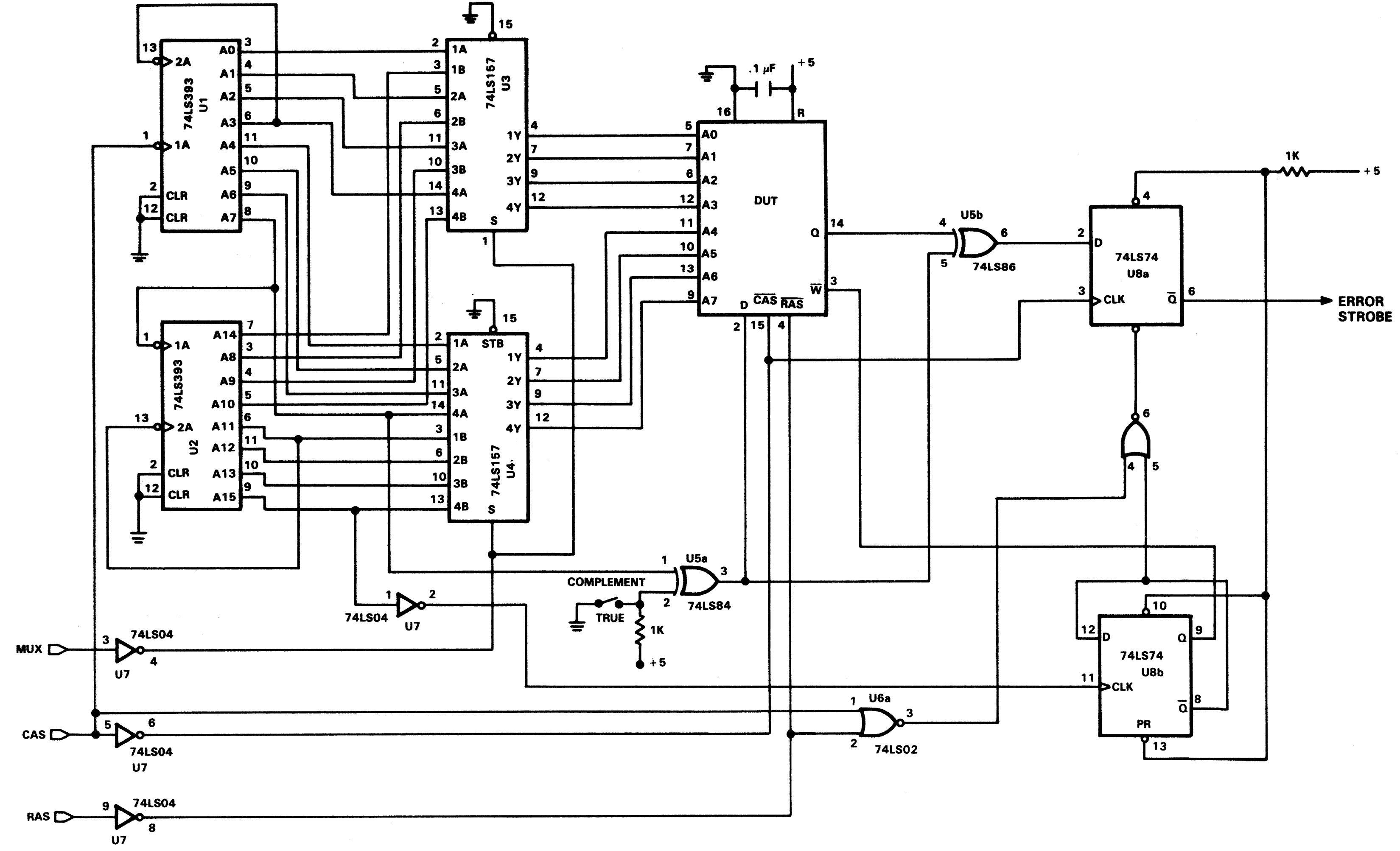


FIGURE I-1 – PORTABLE ALPHA TESTER SCHEMATIC (Continued)

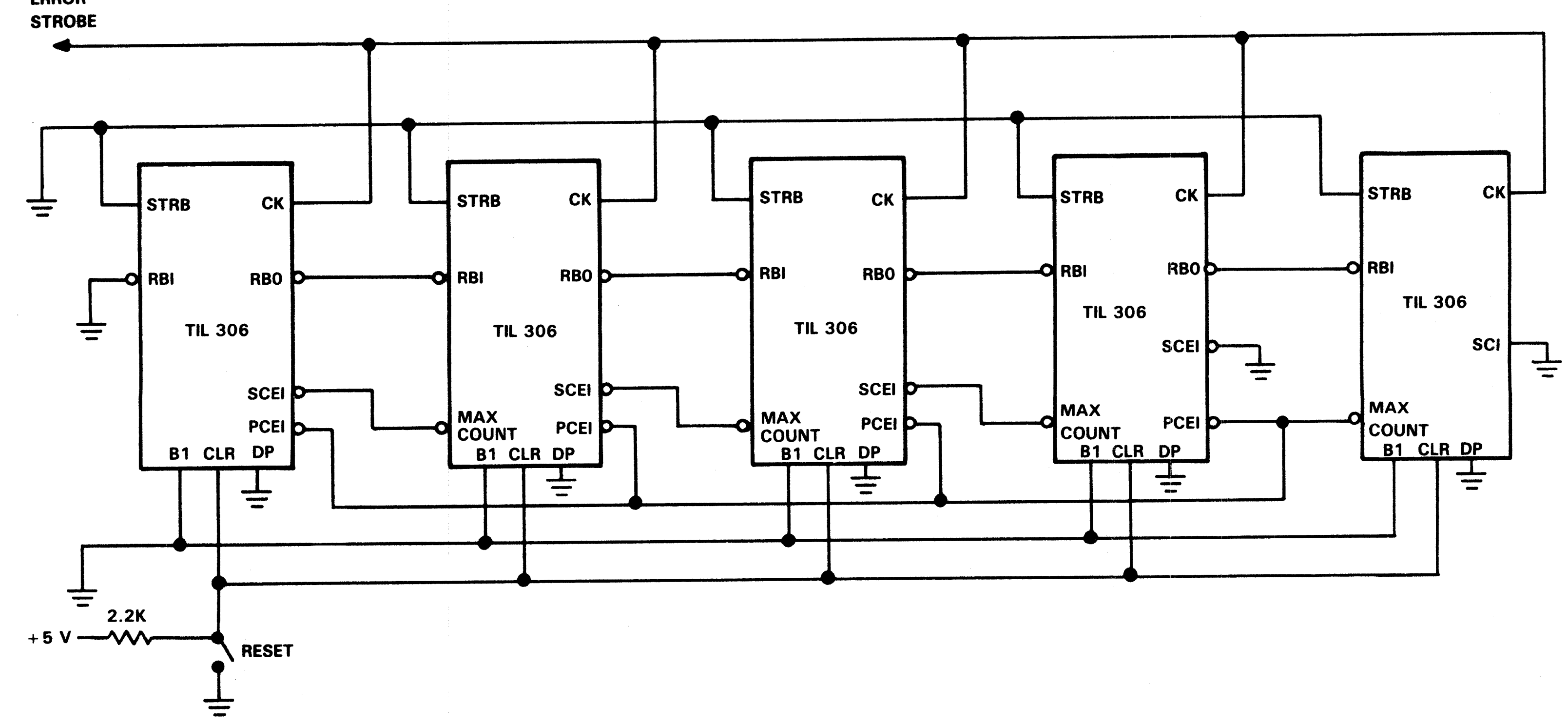


FIGURE I-1 – PORTABLE ALPHA TESTER SCHEMATIC (Concluded)

APPENDIX J

MEMORY SYSTEM TESTER

MEMORY SYSTEM TESTER

GENERAL

The Memory System Tester (MST) is a microprocessor-based board that tests for soft errors. The memory to be tested is located on 16 boards of 64 devices each (1024 total). The refresh feature of the microprocessor supports the DRAMs with an external added eighth refresh bit. The system clock has 229 programmable cycle times that may be changed during system operation by the application programs. These cycle times, combined with the proper instruction sequence, yield refresh rates of from 0.8 microseconds to 147.2 microseconds. A display shows total hours of system operation and also the total error count. In addition, displays are provided to indicate the board and row of a failure as well as the particular failed address and the data that failed. A parallel I/O port is built in to allow communication with an external processor system for logging data or the entry of program changes. The system operates on an uninterruptible power supply for protection from short-term power loss and for isolation from line noise.

The memory boards for the devices under test are configured with eight rows of eight devices with 512K 8-bit words per board. The boards feature an elaborate power supply grid and a decoupling capacitor on each device to assure minimum noise. It is important to make sure that soft errors are generated by alpha particles, not noise. Each block of dynamic memory is accessed as a 32-byte page with a total of 256 pages (eight megabytes) under test.

Addressing for the memory requires eight additional address lines that are latched from the data bus with an output instruction. A15 (processor) from the CPU is used for memory mapping and enabling dynamic memory. Therefore A15 to address the memory under test is obtained from the LSB of these latched addresses. A15 (latched) selects the 32K (low or high) of each 8-bit row to be addressed. A16-A18 select which row (0-7) of each board is addressed and A19-A22 are decoded to provide 1-of-16 board-enable signals. The boards are labeled 0-F. Address lines A0-A14 from the CPU and A15 (latched) from high order address latch are multiplexed to select the location, specific board and row to be addressed. Using this technique any location, 000000-FFFFFF, can be accessed as part of the DRAM array.

The control signals for the DRAMs are generated using the $\overline{MREQ}$, $\overline{RFSH}$, and A15 (processor) signals from the microprocessor. $\overline{RAS}$ must go low on each opcode fetch when the refresh address is output and $\overline{RFSH}$ is low. $\overline{RAS}$ also must go low when A15 (processor) is high and $\overline{MREQ}$ is low to access dynamic memory for a read or write cycle. During a read or write of dynamic memory, $\overline{CAS}$ can go low a minimum of 20 nanoseconds after the falling edge of $\overline{RAS}$, but $\overline{CAS}$ must remain high during refresh. A multiplex select signal to select between the row and column addresses must go low at least 20 nanoseconds after $\overline{RAS}$ goes low to satisfy the row address hold time, but it must have enabled the column address no later than 5 nanoseconds after the falling edge of $\overline{CAS}$. This $\overline{MUX}$ signal is not active during refresh.

The microprocessor's 128-cycle refresh is converted to 256-cycle refresh using the method illustrated in the attached Application Brief. The system multiplexing must pass the low eight address lines to the DRAMs during refresh.

The system clock has 29 programmable cycle times that can be changed during operation either in the system software or from a terminal connected through the MST parallel I/O port. The clock is a 20-megahertz oscillator with a binary divider. The five least-significant bits of the data bus are latched into a binary counter by an output instruction to change the clock speed. Division by 2 and 3 must be prevented because these speeds would exceed the maximum operating speed of the microprocessor. The clock runs at speeds from 200 nanoseconds to 1.6 microseconds. By choosing the correct instruction sequencing and clock frequency, refresh rates can be varied from 0.8 microseconds to 14.2 microseconds.

On-board memory consists of up to 16K EPROM for storage of the operating system and bit patterns, up to 8K of static RAM, and a 256-byte battery-backed CMOS RAM that stores pertinent data in case of long-term power failure. This RAM enables the system to start operation where it left off after power failure. When the system is initialized or starts up from a power-fail, the control program is loaded from the EPROM to the static RAM. This allows the system to operate at higher speeds and allows the user to modify the program during execution using the MST parallel I/O port. Up to 256 soft errors and 256 hard errors can be stored in static RAM. When either of these memory spaces are filled, the data can be dumped to a disc or hard copy through the I/O port.

Communication with the MST is facilitated by a programmable parallel I/O port. The port is configured with one 8-bit input port, one 8-bit output port, and control lines for handshaking with another computer system. When the port is written to by the communication terminal, an interrupt is generated. The interrupt service routine allows the terminal to write data to a memory location, display a byte of data on the MST display, or modify the operating program in static RAM. Data may also be read from memory through the I/O port and either viewed on the terminal CRT, printed on hard copy, or stored on a disc.

A display shows total hours of operation and total error count. The board, row, and address of the error is displayed along with the data that was read incorrectly. Thus the user can pinpoint one of the 64 megabits that has failed.

To protect against short-term power outage, the MST is operated with an uninterruptible power supply (UPS). The system will operate for 1 hour on this supply. The small size of the test system and UPS allows them to be transported to a different supply source in case of long-term power interruptions. The UPS also provides ac power isolated from noise and line voltage fluctuations to help assure valid data.

In case of catastrophic failure, the dc power supply for the system provides a power-fail signal that goes low for 20 milliseconds before the loss of the +5 volt supply. This signal interrupts the processor and initializes a power-down sequence. During this orderly power-down, information is stored in battery-backed RAM to allow testing to resume where it left off when the power failed. When power is restored, the system reads two bytes from the battery-backed RAM and determines if this is a cold start or a start from power-fail. If the proper data is stored, the timer and error displays are restored, and testing goes on from the point of interruption.

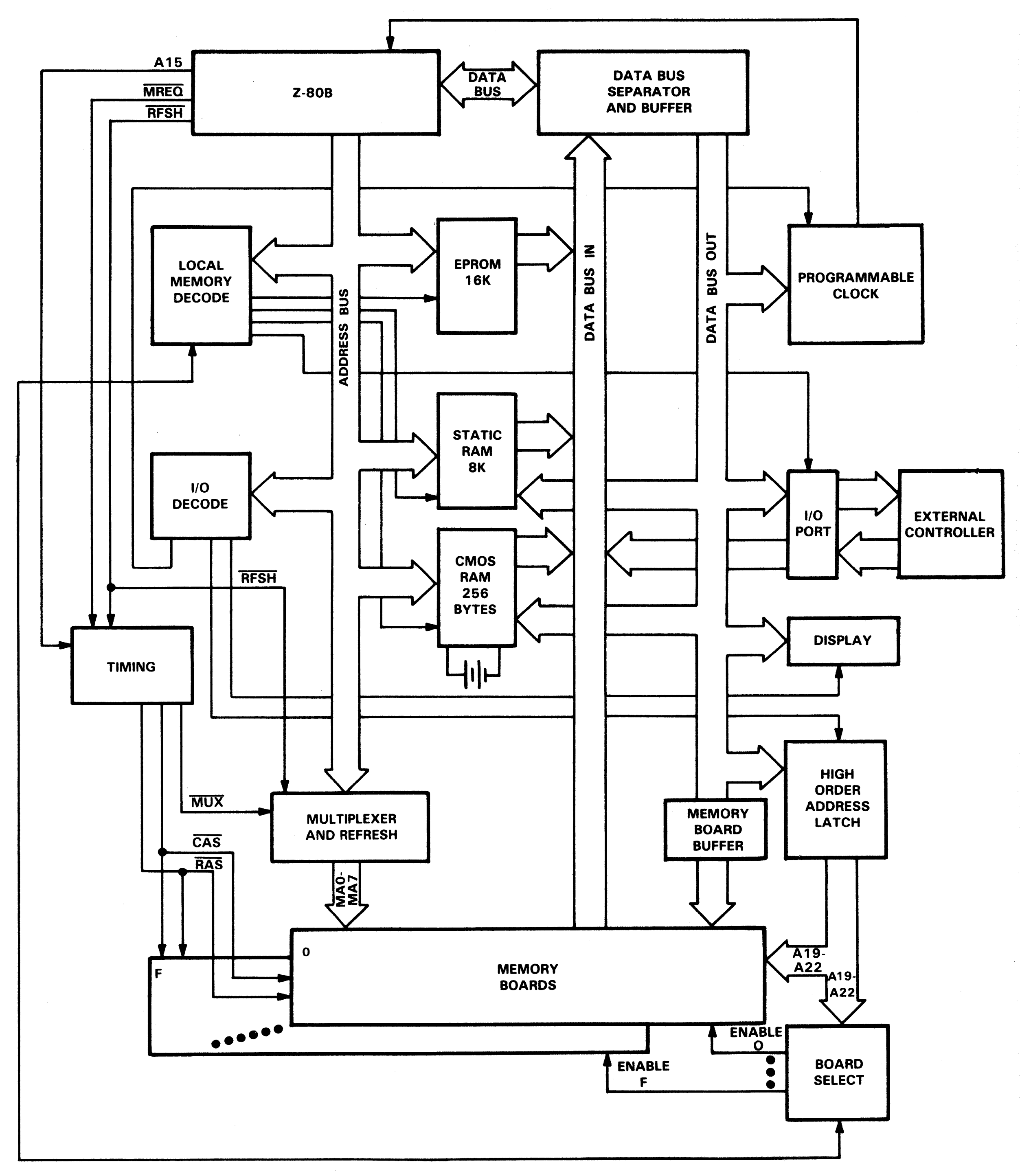


FIGURE J-1 – MST BLOCK DIAGRAM

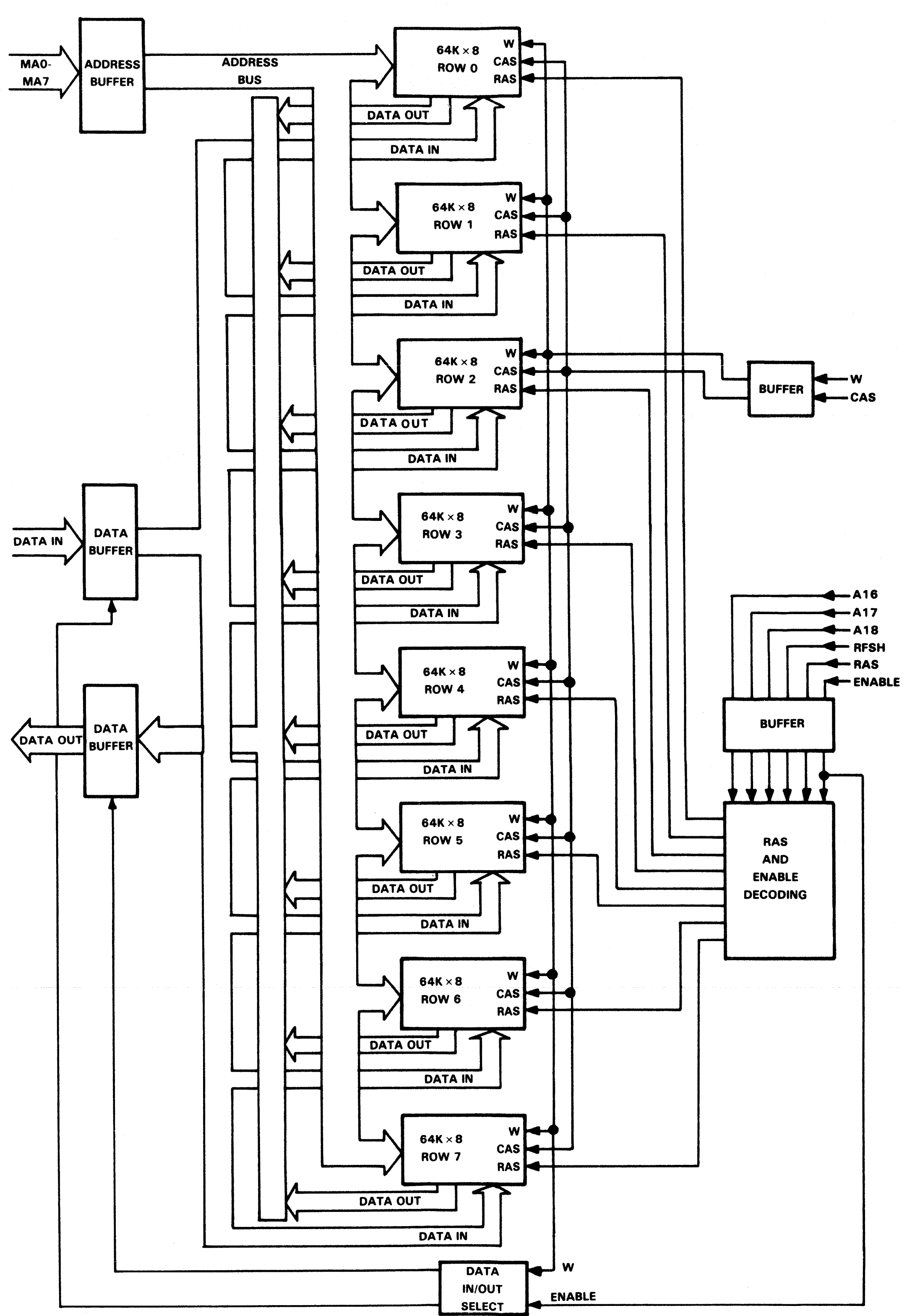


FIGURE J-2 – MST MEMORY BOARD BLOCK DIAGRAM

APPENDIX K

GROUP FUNCTIONS
APPLICATION BRIEFS
TMS 4164 DEVICE SPECIFICATIONS

DRAM APPLICATIONS ENGINEERING GROUP

RESPONSIBILITIES:

Customer technical assistance
Inquiries
Troubleshooting
Correlations

SYSTEM-LEVEL EVALUATIONS:

Soft error rates
Device sensitivities
Quality and reliability

COMPETITIVE TECHNICAL ASSIGNMENTS:

Competitive parts analysis
Support component evaluation

PROMOTIONAL ASPECTS:

Technical articles
Application reports

DETAILED IDENTIFICATION OF NEW PRODUCT OPPORTUNITIES

IN-HOUSE USER-ORIENTED CONSULTANTS TO INTERNAL GROUPS

GATHER, ANALYZE AND VOICE CUSTOMER FEEDBACK

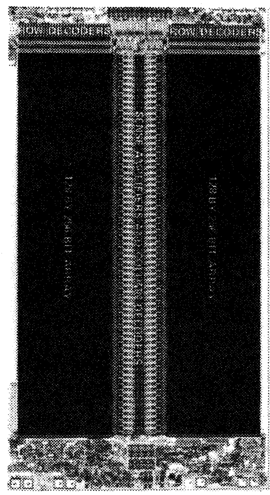
The DRAM Applications Group may be contacted through the Texas Instruments Customer Response Center by dialing 1-214-995-6611 and asking to speak to a MOS Memory Applications Engineer. For correspondence write:

Texas Instruments Incorporated
MOS Memory Applications
P. O. Box 1443
Houston, Texas 77001

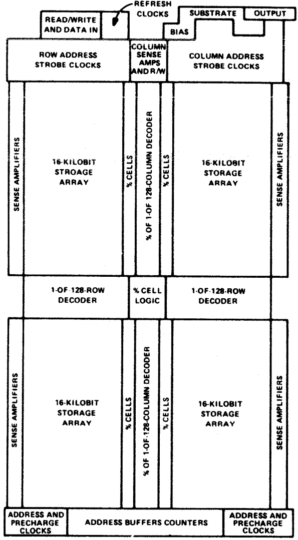
Applications Brief

64K DYNAMIC RAM ARCHITECTURE

TMS 4164



Square Array
- 256 cycles in 4 ms
- 256 sense amps



Dual Array
- 128 cycles in 2 ms
  (2 rows refreshed at a time)
- 512 sense amps

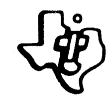
Of the two basic 64K Dynamic RAM architectures illustrated above, TI chose the historically successful industry standard organization for its TMS 4164. This 256-column by 256-row square array results in the following attributes:

- Superior Performance — The 256-cycle approach requires only half the number of sense amplifiers as the 128-cycle approach. Fewer sense amplifiers means lower power dissipation (125 mW typical) and lower junction temperatures (parameters which limit cycle time for many 16K Dynamic RAMs). The TMS 4164-15 is thus able to operate at a dramatically improved 280-ns cycle time versus 375 ns for 16K circuits.

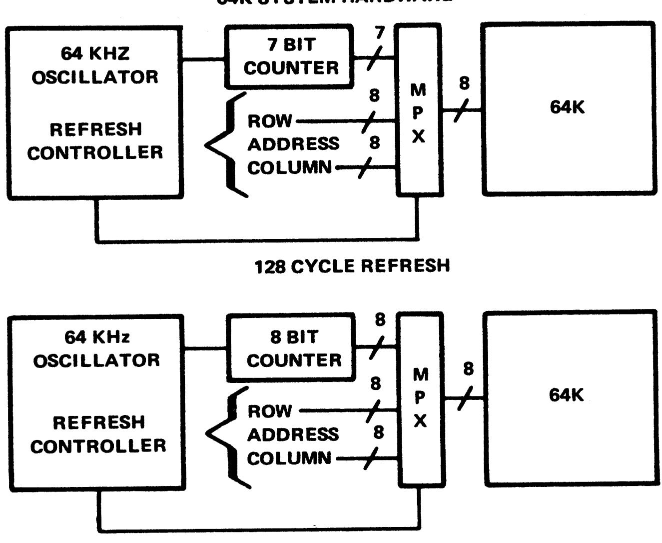
- Improved Reliability — Another advantage resulting from the utilization of only 256 sense amplifiers is the increased chip area which can be devoted to the memory array (array area/bar size = 0.52). This allows each cell to store greater charge and, coupled with the reduced on-chip temperatures, ensures a decreased refresh rate (4 ms per cell versus 2 ms). In addition, current transients and system noise levels are reduced by as much as 2 to 1.

- Low Cost — With only 256 sense amplifiers and reduced on-chip routing, the TMS 4164 organization optimizes bar size and yields a cost-effective, reliable, and producible memory component.

Applications Brief



64K DYNAMIC RAM REFRESH ANALYSIS
SYSTEM DESIGN CONSIDERATIONS



- 8 bit address multiplexing and 8 bit address bus are needed for either 256 or 128 cycle refresh on 64K.
- 128 cycle 64K s require 1 less counter bit (7 vs. 8). This is, however, unlikely to be a practical saving since counters/multiplexers come in 4 and 8 bit multiples.
- 256 cycle/4 ms refresh approach allows the same oscillator timing (64 kHz) to be used when upgrading from 16K s (128 cycle/ 2 ms period).
- Systems designed for 256 cycle 64K s can easily use 128 cycle 64K s.

Compatibility among all 64K Dynamic RAM vendors can be achieved by designing to TI's 4164 64K x 1 Dynamic RAM. The TMS 4164 requires all 256 rows to be refreshed within 4 ms. Competitive 64K DRAMs which are not able to achieve the 256 cycle, 4 ms refresh rate require twice the number of sense amplifiers as the TMS 4164 and half the number of refresh addresses. A 64K DRAM which requires the 128 cycle, 2 ms refresh treats the 256 cycle, 4 ms refresh as two refresh events in 2 ms each.

Simply: 256 cycle in 4 ms = 2 (128 cycle in 2 ms)

The extra address bit, A7, during refresh is treated by these vendors as a don't care situation.

The TMS 4164 has the same refresh rate as the 4116, 16K x 1 Dynamic RAM, which requires 128 rows to be refreshed in 2 ms. Most 4116 based systems already contain the extra refresh counter bit required for upgrading to the 64K. Those implemented with the 74LS393, 8-bit counter already do.

For a given cycle time, say 280 ns, the 256 cycle 4 ms refresh architecture of the TMS 4164 requires the same refresh overhead as the 128 cycle 2 ms approach as can be seen by the following calculations:

$$\text{Refresh overhead} = \frac{\text{refresh cycles in given time}}{\text{available cycles in given time}} = \frac{256 \text{ cycles}}{4 \text{ ms}/280 \text{ ns per cycle}} = \frac{128 \text{ cycles}}{2 \text{ ms}/280 \text{ ns per cycle}} = 1.8\%$$

However, the TMS 4164 provides the user with the following advantages:

- Half the number of sense amplifiers, small chip size, low cost.
- Lower power yielding lower temperature and increased reliability.
- More chip area devoted to memory array allowing greater detectable cell charge and improved performance.

In summary, the TMS 4164 is compatible with 16K DRAMs and other 64K DRAMs since they are all refreshed at the same rate. An extra counter bit A7, introduced to the TMS 4164 during refresh will insure compatibility among all 64K DRAMs.

MOS Memory
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Applications Brief

TMS 4116 VS. TMS 4164 DATA SHEET DIFFERENCES

SPECIFICATION	SYMBOL	−15 4116	−15 4164	−20 4116	−20 4164	−25 4116	−25 4164
Page Mode Cycle Time	$t_{c(P)}$	170	160	225	225	275	275
Read or Write Cycle Time	$t_{c(rd)}$ $t_{c(W)}$	375	260	375	330	410	410
Read-Modify-Write Cycle Time	$t_{c(rdW)}$	375	285	375	345	515	455
Pulse Width, $\overline{CAS}$ High	$t_{w(CH)}$	60	50	80	80	100	100
Pulse Width, $\overline{RAS}$ Low	$t_{w(RL)}$	150	150	200	200	250	250
Column Address Setup Time	$t_{su(CA)}$	−10	−5	−10	−5	−10	−5
Delay Time, $\overline{CAS}$ High to $\overline{RAS}$ Low	t_{CHRL}	−20	0	−20	0	−20	0
Delay Time, $\overline{RAS}$ Low to $\overline{W}$ Low (RMW) Cycle)	t_{RLWL}	120	110	160	130	200	190
Delay Time, $\overline{W}$ Low to $\overline{CAS}$ Low (Early W)	t_{WLCL}	−20	−5	−20	−5	−20	−5
Delay Time, $\overline{CAS}$ Low to $\overline{W}$ Low (RMW Cycle)	$t_{(CLWL)}$	70	60	95	65	125	105
Refresh Period	t_{rf}	2 ms	4 ms	2 ms	4 ms	2 ms	4 ms
Data Hold Time After $\overline{CAS}$ Low	$t_{h(CLD)}$	45	60	55	80	75	110
Data Hold Time After $\overline{RAS}$ Low	$t_{h(RLD)}$	95	145	120	180	160	210
Write Hold Time After $\overline{CAS}$ Low	$t_{h(CLW)}$	45	60	55	80	75	110
Write Hold Time After $\overline{RAS}$ Low	$t_{h(RLW)}$	95	110	120	145	160	195
Column Address Hold Time After $\overline{RAS}$ Low	$t_{h(RLCA)}$	95	95	120	140	160	190

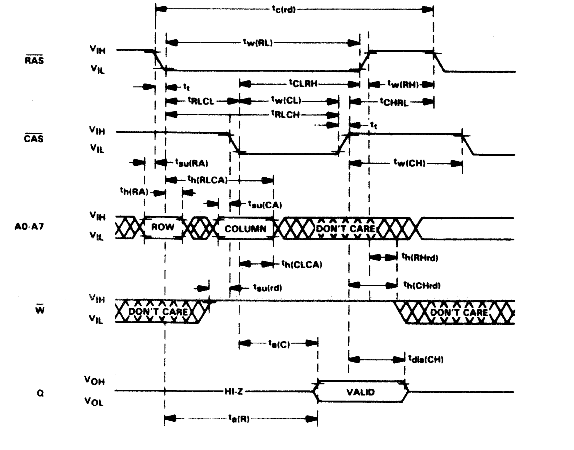
All times are in nanoseconds unless otherwise noted.

Here's what these specification differences mean when upgrading to the TMS 4164.

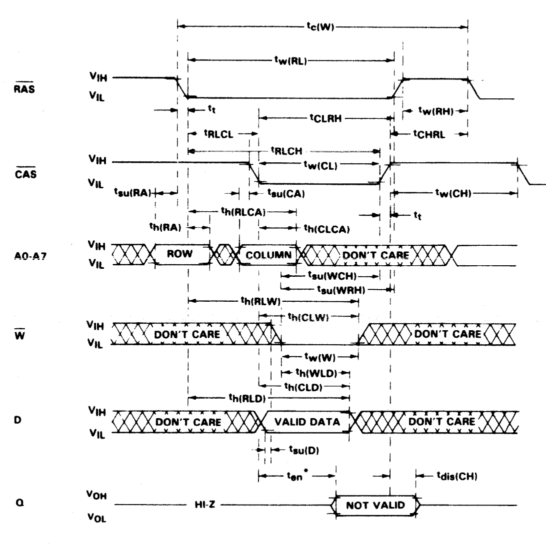
Memory cycle times are reduced in all modes: page mode cycle time as low as 160 ns, read or write cycle time to 280 ns, and read-modify-write cycle time as low as 280 ns.

The TMS 4164 has a 2 cycle, 4 ms refresh which results in the same refresh rate as the 4116's 128 cycle; 2 ms refresh. With the same refresh rate, the faster cycle time of the 64K is the key to lower refresh overhead. The result is refresh overhead reduced from 2.4% (16K) to 1.8% (64K).

read cycle timing



write cycle timing



* The enable time (t_{en}) for a write cycle is equal in duration to the access time from $\overline{CAS}$ ($t_{a(C)}$) in a read cycle, but the active levels at the output are invalid.

Column address setup time is longer on all speed range parts and column address hold time is increased on −20 and −25 parts. This means column address must be presented sooner and held longer when using the TMS 4164.

Data In, Write Command, and RAS low have longer hold times with the 4164. The removal of these signals is late in the cycle and usually a "cleanup" operation. For this reason, the longer hold times do not affect system performance as the access time from $\overline{RAS}$ remains the same as the 4116.

Other differences include a shorter delay time from $\overline{RAS}$ and $\overline{CAS}$ to $\overline{W}$ low on the read-modify-write cycle and a shorter delay time from $\overline{W}$ low to $\overline{CAS}$ low on an early write cycle. These differences are expected with the shorter cycle times of the 4164.

Overall the TMS 4164 specifications show significant improvements over the TMS 4116. These improvements mean upgrading to the 4164 not only yields a denser memory layout but also significant speed advantage.

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Applications Brief

TMS 4164 SYSTEM POWER REQUIREMENTS

The TMS 4164 dissipates considerably less power than the TMS 4116. On a per-bit basis, the average operating power of the 64K is less than one-eighth of the 16K. To take advantage of this low power dissipation, it is necessary to calculate the maximum average current a memory system will consume. Worst-case power supply requirements can be determined through the use of the following equations:

$$I_{DD} = N\,[R \times I_{DD3} + (1\text{-}R)\,(A \times I_{DD1} + (1\text{-}A)\,I_{DD2})]$$

where I_{DD} = maximum average current of system
N = number of devices in system
R = refresh overhead
A = relative time memory is active
I_{DD3} = average refresh current (Table 1 or Figure 1)
I_{DD2} = average standby current (Table 1)
I_{DD1} = average active current (Table 1 or Figure 1)

Parameter A is calculated by dividing the word size by the number of devices in the system. This assumes only one word of memory can be accessed at one time.

$$A = \frac{\#\text{ devices/word}}{\#\text{ devices/system}}$$

Parameter R is the ratio of the time required to refresh the memory to the time the memory is available to be accessed. This can be calculated by multiplying the cycle time and refresh rate.

$$R = \text{cycle time} \times \text{refresh rate}$$

As an example, examine a system with 64 4164's organized as 512 kilobytes of memory. Assume cycle time of 350 ns and minimum refresh rate (64 kHz).

$$N = 64$$
$$A = \frac{8}{64} = .125$$
$$R = 350 \times 10^{-9} \times 64 \times 10^{3} = .022$$
$$I_{DD} = 37 \times 10^{-3}\ \text{A}$$
$$I_{DD2} = 5 \times 10^{-3}\ \text{A}$$
$$I_{DD3} = 32 \times 10^{-3}\ \text{A}$$

TABLE 1 – I_{DD} ELECTRICAL CHARACTERISTICS FOR TMS 4164–20

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{DD1}	Average operating current during read or write cycle	t_c = minimum cycle		24	34	mA
I_{DD2}	Standby current	After 1 memory cycle, $\overline{RAS}$ and $\overline{CAS}$ high		3.5	5	mA
I_{DD3}	Average refresh current	t_c = minimum cycle $\overline{RAS}$ low, $\overline{CAS}$ high		19	26	mA

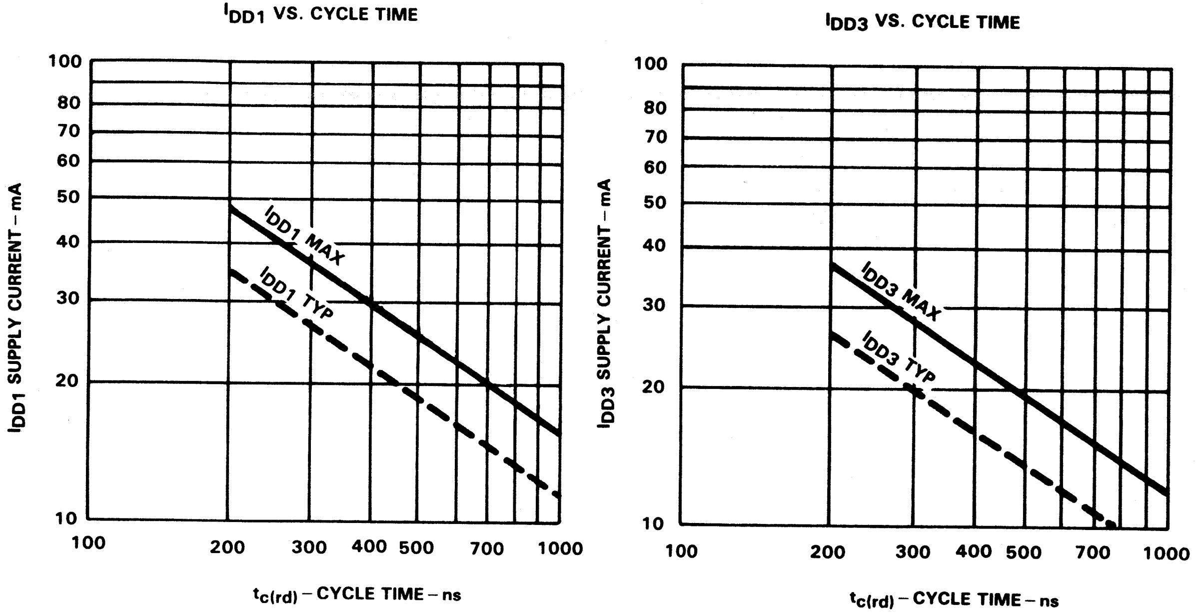


FIGURE 1 – I_{DD} vs CYCLE TIME

Substituting into original equation

$$
\begin{aligned}
I_{DD} &= 64\ [.022\ (26 \times 10^{-3}) + (1-.022)\ [(.125)\ (34 \times 10^{-3}) + (1-.125)\ (5 \times 10^{-3})]] \\
&= 64\ [5.72 \times 10^{-4} + .978\ [4.25 \times 10^{-3} + 4.375 \times 10^{-3}]] \\
&= 64\ [5.72 \times 10^{-4} + 8.435 \times 10^{-3}] \\
&= 5.77 \times 10^{-1} A = 577\text{ mA maximum average current}
\end{aligned}
$$

To determine the maximum average current with the system on standby, let A = 0

$$
\begin{aligned}
I_{DD} &= 64\ [.022\ (26 \times 10^{-3}) + (1-.022)\ [0 + 5 \times 10^{-3}]] \\
&= 64\ [5.72 \times 10^{-4} + 4.89 \times 10^{-3}] \\
&= 3.50 \times 10^{-1} = 350\text{ mA maximum average current standby mode.}
\end{aligned}
$$

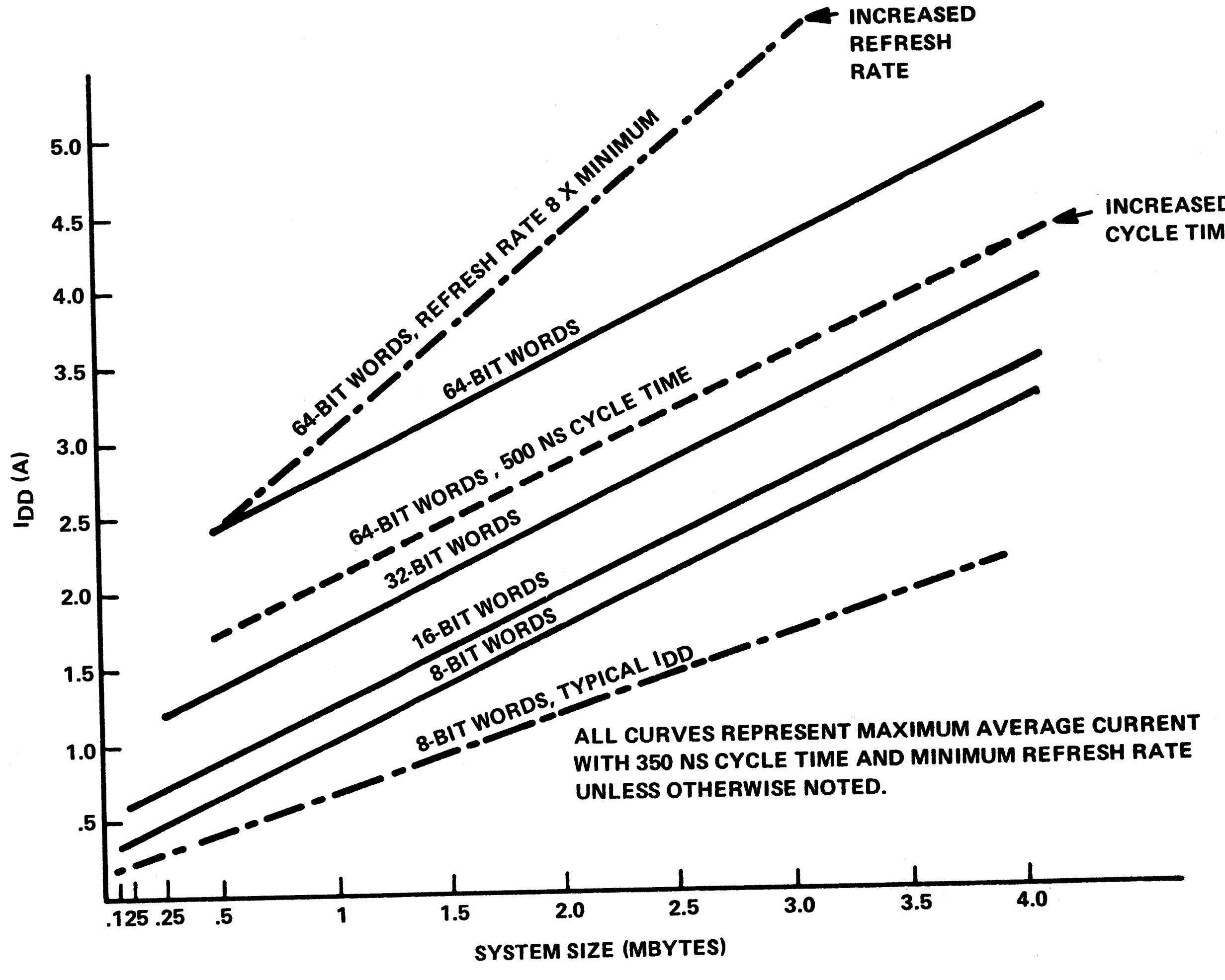


FIGURE 2 – 100%-ACTIVE I_{DD} vs SYSTEM SIZE

The graph in Figure 2 was plotted using the equation for maximum average current. This graph shows the maximum amount of current a memory system could draw with the memory organized in different word sizes. The graph also shows the effect of increasing cycle and refresh time on system power requirements. Finally, the graph shows the difference between maximum average current and typical average current.

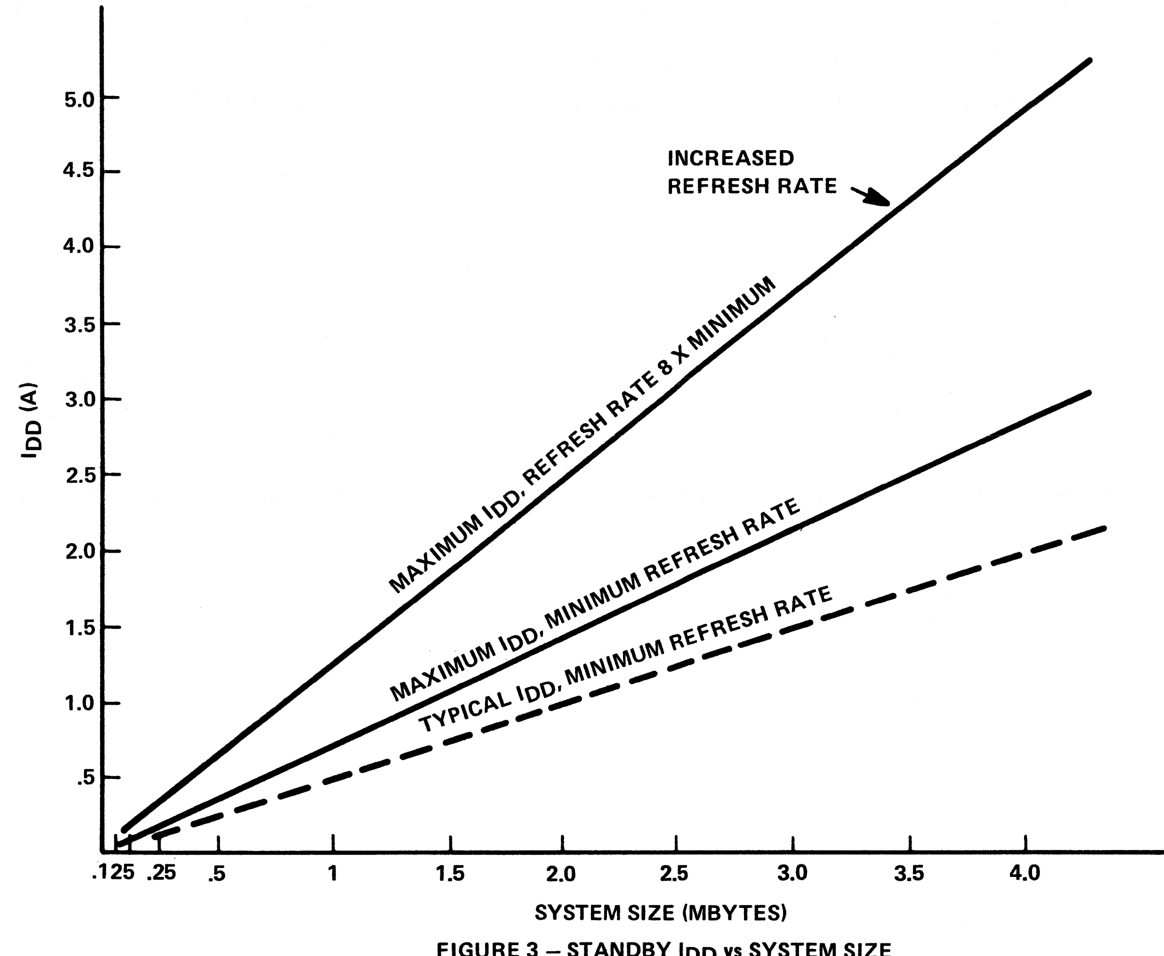


FIGURE 3 — STANDBY I_{DD} vs SYSTEM SIZE

Figure 3 shows the current necessary to operate various system sizes in the standby mode. The current required at refresh rate 8X higher is also plotted to show the effect of refresh rate on system power requirements. The dotted line shows the calculations of typical average current using minimum refresh time.

These calculations make it possible to properly match power supply ratings to memory system requirements. They are also necessary in designing a battery-backup system for which worst-case standby current requirements would be needed. These calculations emphasize the low power requirements of the TMS 4164 in a system environment.

MOS Memory
Applications Engineering

Applications Brief

TMS 4164 PRINTED CIRCUIT BOARD LAYOUT

PIN 1 PIN 9

COMPONENT SIDE

SOLDER SIDE

A7 J2

J1

$\overline{CAS}$

$\overline{W}$

A6

$\overline{RAS}$

A3

A0

A4

A2

A5

A7 A1

J2

J1

(+12 – 4116 / +5 – 4164) V_{DD}

(GND) V_{SS}

← (+5 V 4116)

(GND – 4164 / –5 V – 4116)

FIGURE 1 – UNIVERSAL LAYOUT FOR DYNAMIC MEMORY (SHOWN 2X)

Figure 1 is an X-Ray view of a universal memory layout that can use either dynamic RAMs requiring three supply voltages, such as the 4116 or those requiring only a single 5-volt supply, such as the 4164. The spacing between chips is large enough to facilitate different capacitor placement for each layout type.

To use this layout for 4116's, jumpers would be placed at J1 to connect pin 9 to +5 volts. The bus that is connected to pin 1 should be at –5 volts for 4116's. Capacitors would be placed between –5 volts and ground in the spaces provided on every other chip (A). Remaining chips would have capacitors placed between the +12-volt line and ground (B). Bypass capacitors for the +5-volt line are not as critical so they can be placed around the periphery of the array.

A different jumper setting and capacitor placement must be used for a 4164 array. Jumpers J2 would connect pin 9 to A7 and J1 would be left open. Pin 1 no longer needs to be –5 volts since pin 1 on the 4164 is not connected internally. This line could be grounded to reduce crosstalk between $\overline{CAS}$ and the power supply line. Capacitors can now be placed between +5 volts and ground (B) on every chip to yield a quiet memory layout.

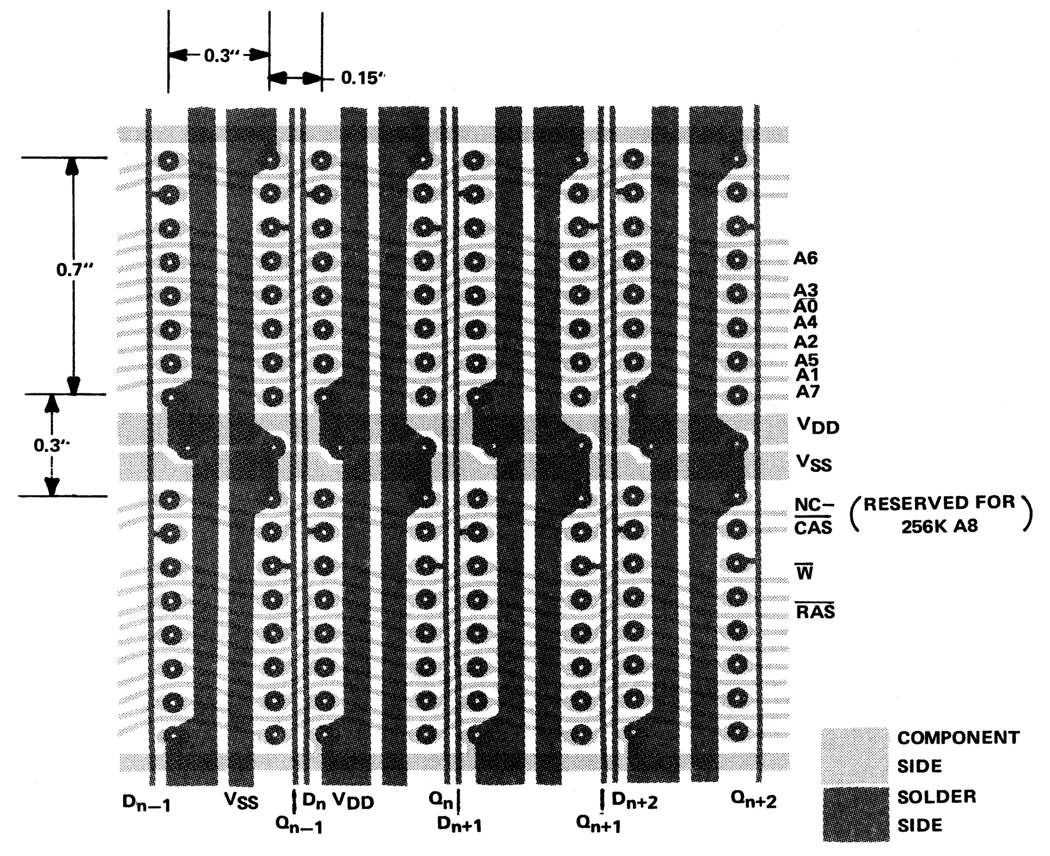


FIGURE 2 – PC BOARD LAYOUT FOR TMS 4164
(SHOWN 2X)

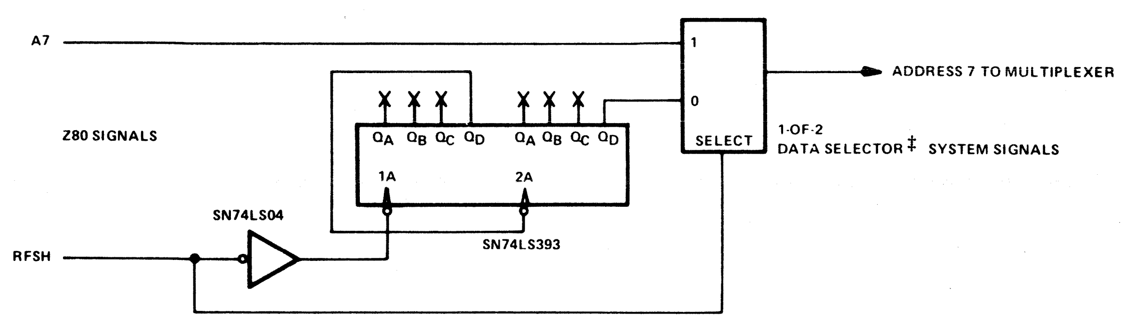
Figure 2 shows a high density PC board layout for the TMS 4164. This layout features gridded power supply buses and one bypass capacitor per dynamic RAM to achieve low-noise supply voltages. The spacing used would allow 64-4164's (512 Kilobytes) to occupy an area of 3.6" x 8" (28.8 square inches). Even smaller spacing between chips could be used if capacitors and sockets were carefully chosen.

Both layouts (Figure 1 and Figure 2) would also need some type of bulk decoupling to filter low frequency noise from the power supplies. The array in Figure 1 would probably not be used in arrays of greater than 32 chips for two reasons. First the added capacitance of the wide trace would increase the rise and fall time of the signal on pin 9. Secondly, the greater spacing between chips means the layout uses more board area. For arrays larger than 32 chips it would be worthwhile to design a separate board for 4116's and 4164's. For a smaller board in a system in which memory requirements would be expected to increase, the universal layout could save the step of redesigning the memory board.

MOS Memory
Applications Engineering

Applications Brief

256-CYCLE REFRESH CONVERSION



‡ This may be implemented in descrete logic, with an SN74LS157 or other scheme.

CIRCUIT TO CONVERT Z80 128-CYCLE REFRESH TO 256-CYCLE REFRESH REQUIRED BY TMS 4164

Adding the circuit above to Z80-based systems increases availability and competitive pricing among those vendors who have announced 64K dynamic RAMs[1] including

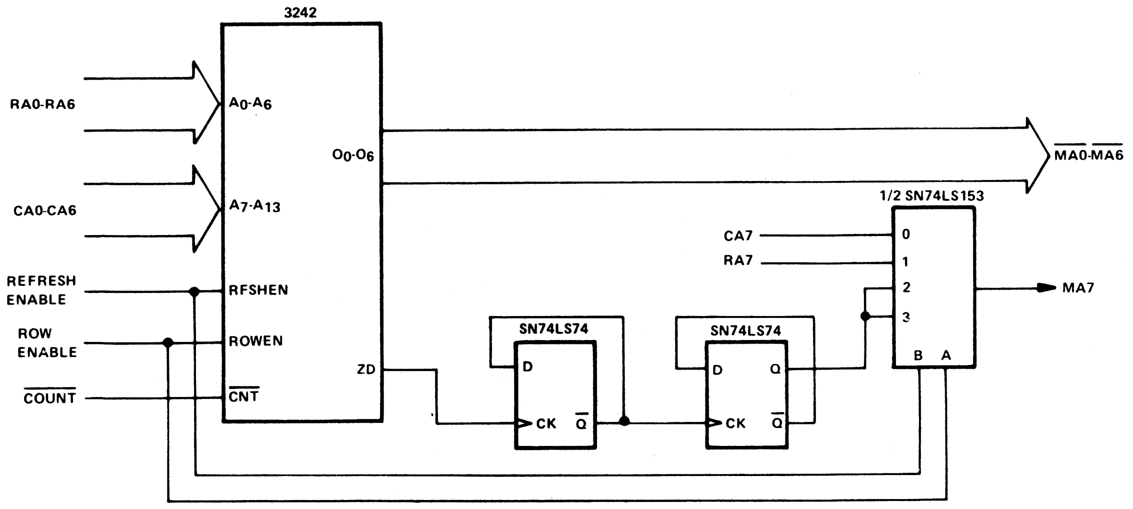
* TEXAS INSTRUMENTS
— Fairchild
— Inmos
— National
— Signetics

Z80 users who are considering an upgrade in dynamic memory from 16K to 64K have much to gain by modifying the Z80 128-cycle refresh. The circuit shown above converts the Z80 128-cycle refresh to the 256-cycle refresh required by TI's TMS 4164 64K dynamic RAM. Designing in the 256-cycle refresh results in broader choice of 64K dynamic memory available to the designer. Designing with only 128-cycle capability severely limits the potential sources for 64K dynamic RAMs.

Adding the circuit shown above to the Z80-based system also allows the designer to take advantage of the TMS 4164's low cost and low power dissipation that result from using only half as many sense amplifiers as the 128-cycle approach.

[1] Electronics, May 22, 1980

EXPANSION OF 3242 FOR 256-CYCLE REFRESH



RA0-RA7 - ROW ADDRESS

CA0-CA7 - COLUMN ADDRESSES

$\overline{MA0}$-$\overline{MA6}$ - MEMORY ADDRESSES (INVERTED)

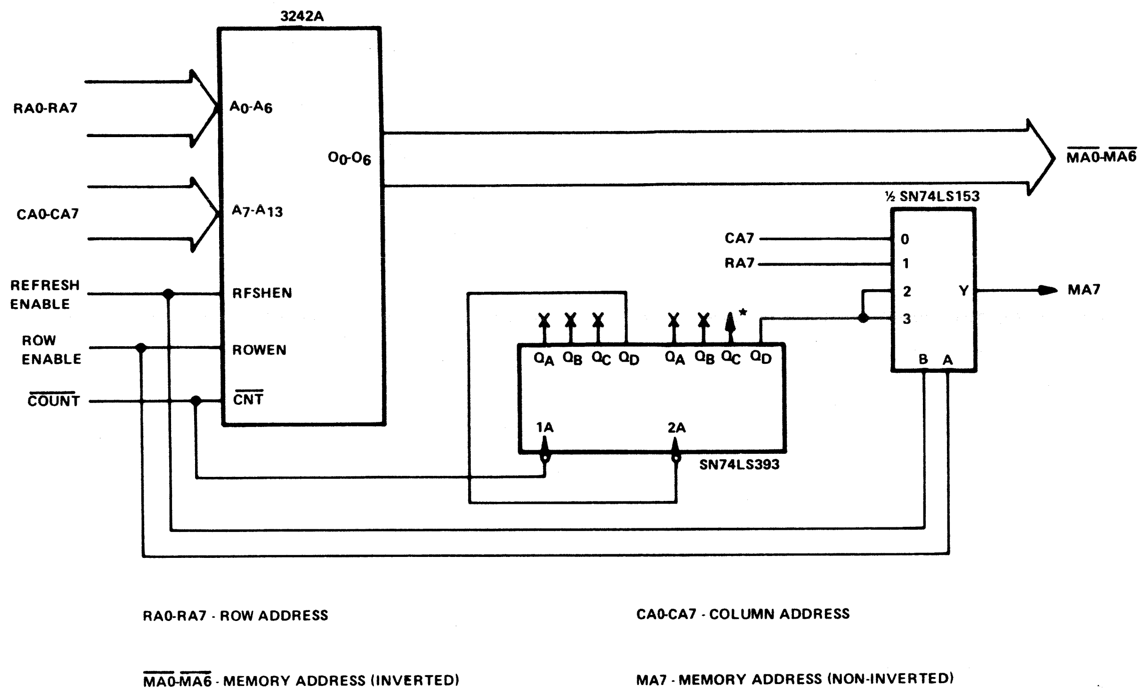
MA7 - MEMORY ADDRESS (NON-INVERTED)

Adding the above circuit to those systems which utilize a 3242 allows the use of 256-cycle-refresh parts. The circuit on the following page may also be incorporated into designs using the 3242A where the zero-detect output is not available.

These designs are presented to demonstrate possible implementation, however, particular system requirements may suggest alternate circuits to optimize component layout.

NOTE: The SN74LS153 may be replaced with an SN74LS352 to obtain inverted signal for all memory addresses.

EXPANSION OF 3242A FOR 256-CYCLE REFRESH



RA0-RA7 - ROW ADDRESS

CA0-CA7 - COLUMN ADDRESS

$\overline{MA0}$-$\overline{MA6}$ - MEMORY ADDRESS (INVERTED)

MA7 - MEMORY ADDRESS (NON-INVERTED)

★ This output may be used to implement 256-cycle refresh for 3232 devices in conjunction with the other half of the SN74LS153.

In summary, these circuits show how to convert a system to a design with maximum flexibility that can use either 128-cycle or 256-cycle 64K dynamic RAMs. Meeting this requirement allows the use of any 64K RAM which will ultimately result in the lowest cost and most reliable system.

Applications Brief

TTL ADDRESS DRIVERS AND LINE TERMINATION IN MOS MEMORY ARRAYS

State-of-the-art MOS memory logic levels are compatible with the voltage levels of TTL logic families. MOS inputs require very little current, so that a standard TTL output is capable of driving up to 32 memory devices on a bus line. However, the extremely high speeds of the TTL devices (from 2 to 3 nanoseconds transition time) can induce ringing due to transmission-line effects even on printed circuit lines only 7 inches long.

A printed circuit trace 0.015 inches wide on 0.062-inch double-sided board can be represented by a transmission line with distributed capacitance (C_D) and inductance (L_D) of 15 picofarads and 0.2 microhenries per foot. From this, we can calculate the characteristic impedance of the transmission line.

$$Zo = \sqrt{\frac{L}{C}} = \sqrt{\frac{0.20 \times 10^{-6}}{15 \times 10^{-12}}}$$
$$= 115\ \Omega$$

Adding an MOS memory input (C_I = 5 picofarads) every half inch, as shown in Figure 1 below, will increase the distributed capacitance effectively to 135 picofarads per foot.

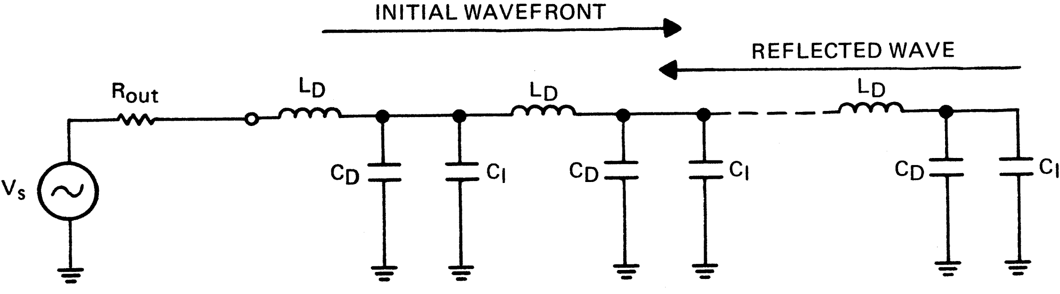


FIGURE 1 – EQUIVALENT CIRCUIT OF MEMORY ARRAY

Characteristic impedance of the transmission line can then be calculated in the following manner:

$$Zo = \sqrt{\frac{0.20 \text{ X } 10^{-6}}{135 \times 10^{-12}}} = 39\ \Omega$$

The equivalent impedance of the line with 1 memory input every half inch is only 39 Ω.

Whenever a discontinuity occurs in a transmission line, a portion of the signal traveling down the line will be reflected. These reflections add to the original waveform and cause distortion of the rising and falling edges in the form of plateaus, undershoot, and ripple.

One method that could be used to reduce this distortion is parallel termination. This involves tying a resistor between a point at the end of the array and another voltage source as shown in Figure 2.

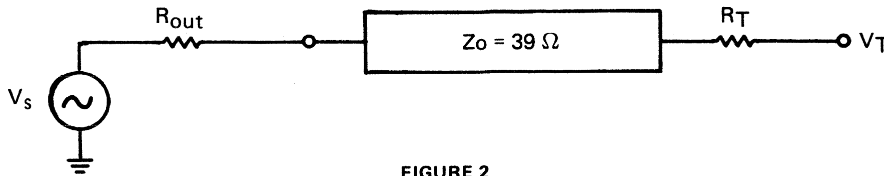


FIGURE 2

Typically, +5 V would be used for V_T because it is always available in systems using TTL devices. The problem with this type of termination is the amount of current required to pull the line low. For R_T = 39 Ω, the current calculations for a low level would be:

$$I_{OL} = \frac{5\text{ V} - 0.4\text{ V}}{39\ \Omega} = 118\text{ mA}$$

This obviously eliminates this configuration for such a low value of terminating resistor. Even if V_T = 2 V, the current values are still not acceptable for TTL drivers.

$$I_{OL} = \frac{2\text{ V} - 0.4\text{ V}}{39\ \Omega} = 41\text{ mA}$$

$$I_{OH} = \frac{2\text{ V} - 2.4\text{ V}}{39\ \Omega} = 10\text{ mA}$$

The alternative in this case is a series terminator at the source, as shown in Figure 3. This places a resistor directly in series with the TTL output.

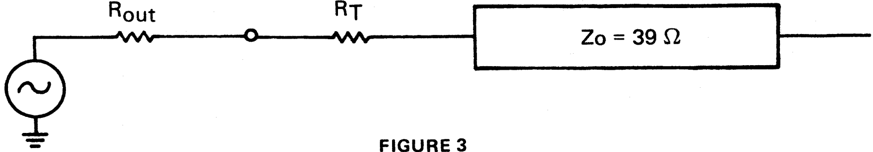


FIGURE 3

This configuration does two things. First, the added series resistance slows the rise and fall times of the signals driving the memory array. Also, the series resistor matches the TTL output to the transmission line. With R_T in place, reflections will still occur because of the discontinuity at the end of the line, but primary reflections will be dissipated by the terminating resistor so secondary reflections will not occur. The effect of the primary reflections can be minimized by the proper selection of R_T. The resistor in series does not add to the dc current requirement to drive the line.

A perfect match is not possible, however, because of the different output impedances of the driver at high and low levels. R_{out} is approximately 10 Ω in the low state and approximately 80 Ω in the high state. Considering the different output impedances and the increased rise and fall times caused by the added resistance, the best value of R_T is chosen by trial and error.

Finally, consideration must be given to the routing of the lines through the array. If the driver is driving more than one row so that several parallel branches are formed, care should be taken to keep each of the paths to the same length. The arrangement shown in Figure 4 is one way to achieve this in a multiple row layout.

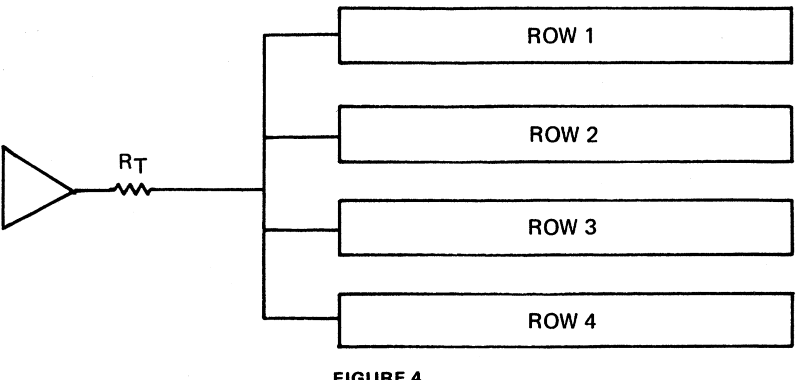
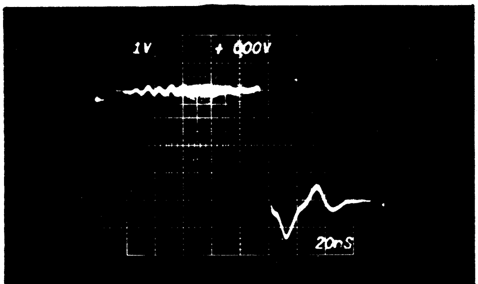


FIGURE 4

As an example, a memory system with 32 TMS4116's arranged as 4 rows by 8 devices was driven with a SN74S240 driver and a series terminator. The responses for no termination; 15 Ω, 22 Ω, 33 Ω, 47 Ω, and 68 Ω are shown in Figures 5 through 10. The high-to-low transitions showed undershoot and ringing that decreased as the terminator increased. The best high-to-low transition; (considering undershoot, ringing, and edge time) was achieved at 47 Ω. The low-to-high response looked good even with no termination. This can be explained best by the fact that the TTL output impedance in the high level is 80 Ω. As the termination increased, the low-to-high transition time increased.



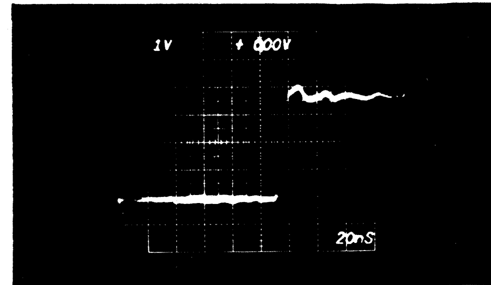
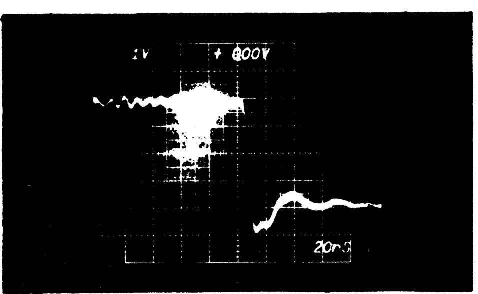


FIGURE 5 — NO TERMINATION



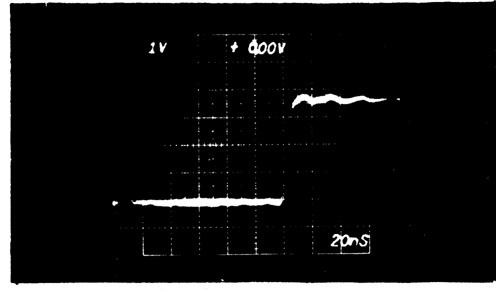
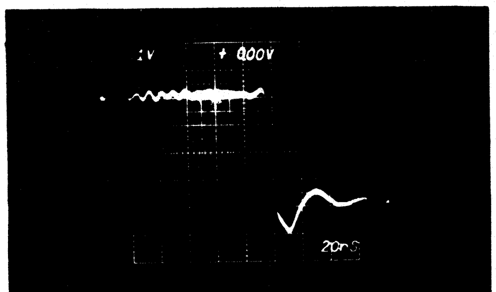


FIGURE 6 — 15-Ω SERIES TERMINATION



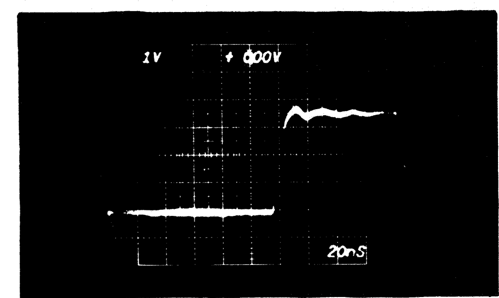
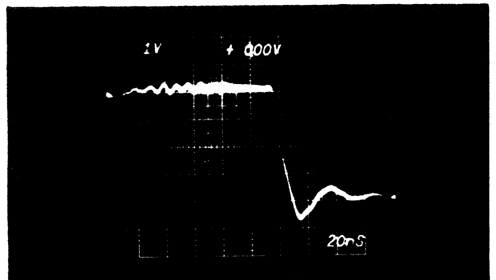


FIGURE 7 – 22-Ω SERIES TERMINATION



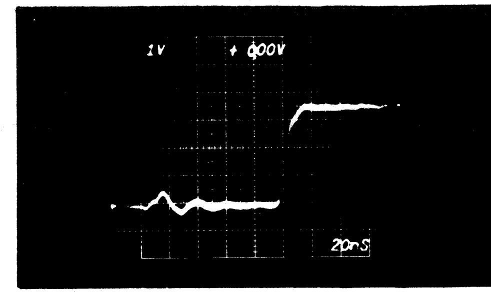
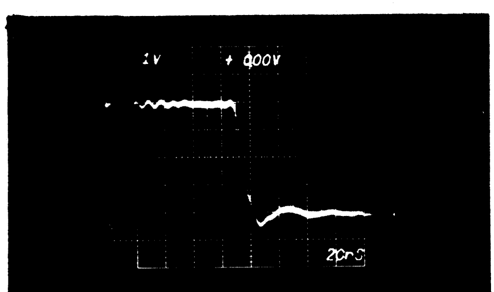


FIGURE 8 – 33-Ω SERIES TERMINATION



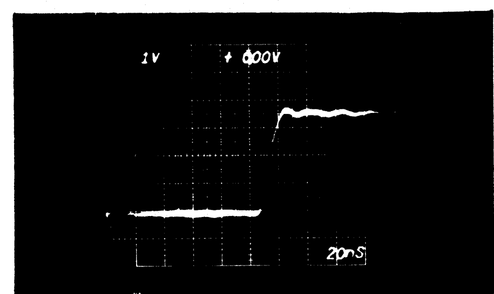
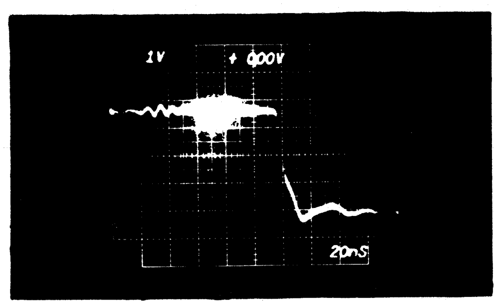


FIGURE 9 – 47-Ω SERIES TERMINATION



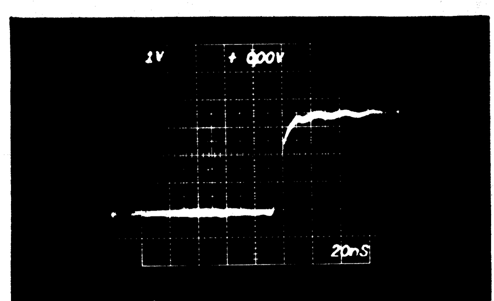


FIGURE 10 – 68-Ω SERIES TERMINATION

The photographs in this article show how the series terminating resistor affects both the rising and falling edges in a typical system. Since every layout will vary because of type of memory used, number of devices in the array, and actual memory layout, the method of trial and error should be followed for each memory design.

MOS Memory
Application Engineering

Applications Brief

TMS 4164
INTERNAL TOPOLOGY

For complete testing and characterization of the TMS 4164 with respect to cell pattern sensitivity, it is necessary to know its true address bit significance. The sixteen address bits required to access the 65,536 cell locations are multiplexed onto eight inputs as eight row (entered by falling edge of $\overline{RAS}$) and eight column (entered by falling edge of $\overline{CAS}$) addresses.

The pinout of the TMS 4164 (Figure 1A) shows these address lines as A0 – A7. The pinout uses this particular address arrangement to maintain compatibility to earlier (4K and 16K) Dynamic RAM memories, although the TMS 4164 uses a different binary weighting on these lines internally. In a system there is no particular advantage to this order of addressing since the device requires no special sequencing to read or write a given memory location.

The bit map of the TMS 4164 array can be obtained using the true address bit significance as shown below for both row and column addressing.

DESIRED ROW OR COLUMN ADDRESS		WEIGHT	TMS 4164 PIN NAME	PIN #
(MSB)	A7	2^7	A7	9
	A6	2^6	A0	5
	A5	2^5	A2	6
	A4	2^4	A1	7
	A3	2^3	A5	10
	A2	2^2	A4	11
	A1	2^1	A3	12
(LSB)	A0	2^0	A6	13

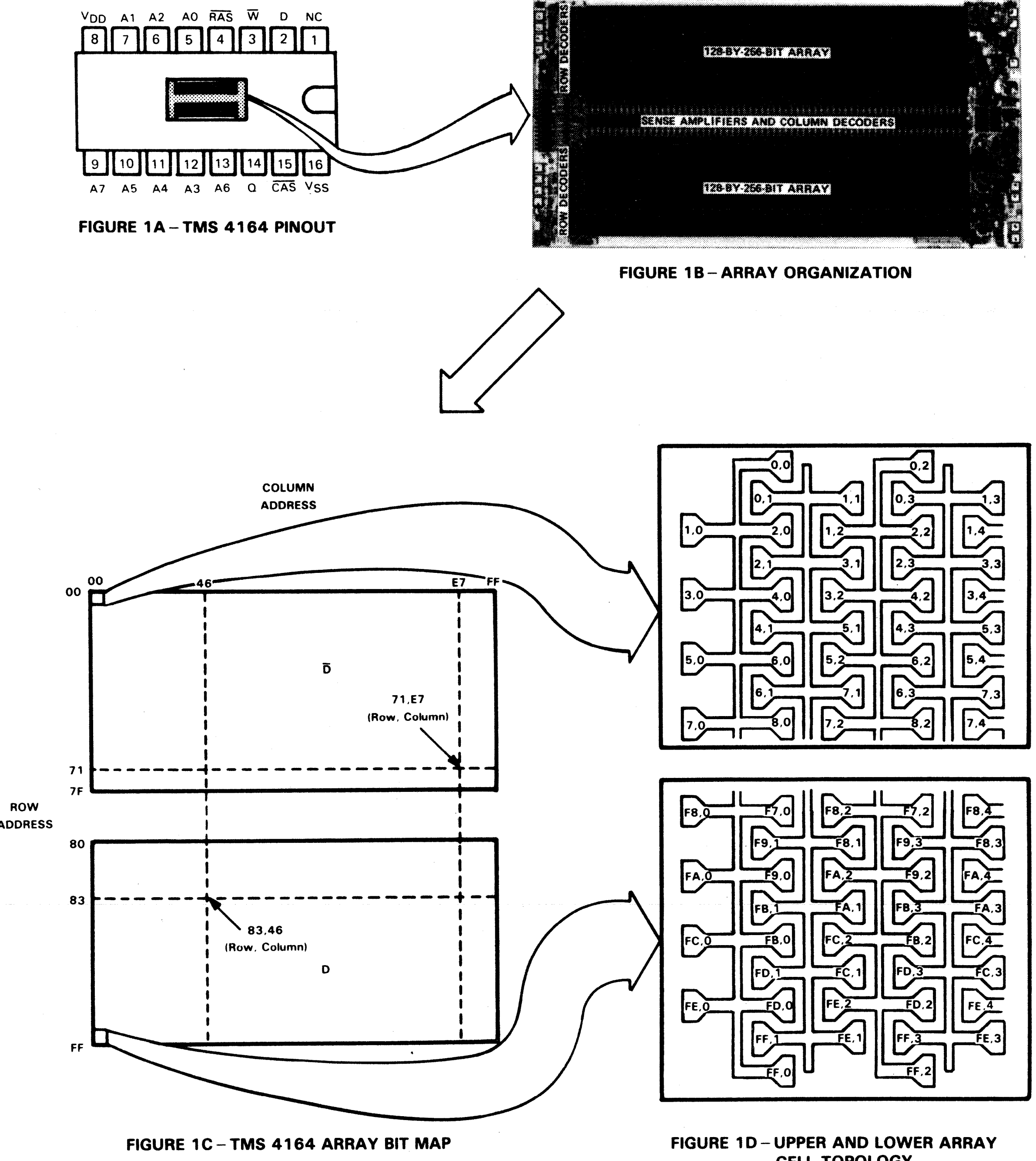


FIGURE 1A – TMS 4164 PINOUT

FIGURE 1B – ARRAY ORGANIZATION

FIGURE 1C – TMS 4164 ARRAY BIT MAP

FIGURE 1D – UPPER AND LOWER ARRAY CELL TOPOLOGY

Figure 1A shows the chip pinout, Figure 1B is a closeup of the array, Figure 1C shows the bit map for the rows and columns, and Figure 1D is a closeup of the cell topology in the array.

Internally the cells are arranged so as to maximize the cell size within the available area. This layout is shown in Figure 1D. The neighboring cells surrounding any particular cell are considered here for their degree of influence on that cell. Each cell has two nearest neighbor cells located in an adjacent column. These have a greater degree of influence upon the cell than do the near neighbors. The near and nearest neighbors for a specific cell can be obtained using the algorithm given below and Figure 1D.

Let (R, C) represent any cell location where R = row address and C = column address.

If row and column addresses are either both even or both odd:

Row Address $\leq 7F_H$			Row Address $\geq 80_H$	
		Nearest Neighbors		
R−2	C+1		R−2	C−1
R+0	C+1		R+0	C−1
		Near Neighbors		
R−2	C+0		R−2	C+0
R+2	C+0		R+2	C+0
R−1	C+2		R−1	C−2

If row and column addresses are neither both even nor both odd:

Row Address $\leq 7F_H$			Row Address $\geq 80_H$	
		Nearest Neighbors		
R+0	C−1		R+0	C+1
R+2	C−1		R+2	C+1
		Near Neighbors		
R−2	C+0		R−2	C+0
R+2	C+0		R+2	C+0
R+1	C−2		R+1	C+2

Note that the algorithm changes for each half of the array due to the fact that the top half is laid out as the mirror image of the bottom half. Data in the top half of the array (as shown in Figure 1C) is stored in inverted form (absence of charge = 1), while data in the lower half is stored in true form (charge = 1). Therefore, row address bit seven is the bit which selects between true and inverted array. This may be transformed using the circuit shown in Figure 2 to compensate for this internal data inversion.

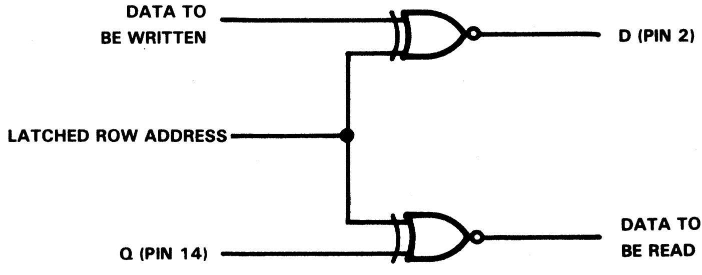


FIGURE 2 – CIRCUIT FOR COMPENSATION OF INTERNAL DATA INVERSION

MOS Memory
Applications Engineering

MOS
LSI

TMS 4164 JDL, NL, FPL
65,536-BIT DYNAMIC RANDOM-ACCESS MEMORY

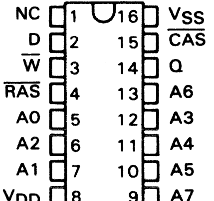
JULY 1980 — REVISED MAY 1982

- **65,536 X 1 Organization**
- **Single +5 V Supply (10% Tolerance)**
- **JEDEC Standardized Pin Out in Dual-In-Line Packages**
- **Upward Pin Compatible with TMS 4116 (16K Dynamic RAM)**
- **Performance Ranges:**

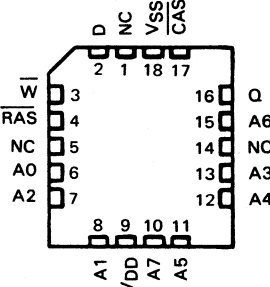
	ACCESS TIME ROW ADDRESS (MAX)	ACCESS TIME COLUMN ADDRESS (MAX)	READ OR WRITE CYCLE (MIN)	READ, MODIFY, WRITE CYCLE (MIN)
TMS 4164-12	120 ns	75 ns	230 ns	260 ns
TMS 4164-15	150 ns	100 ns	260 ns	285 ns
TMS 4164-20	200 ns	135 ns	330 ns	345 ns
TMS 4164-25	250 ns	165 ns	410 ns	455 ns

- **Long Refresh Period . . . 4 milliseconds**
- **Low Refresh Overhead Time . . . As Low As 1.8% of Total Refresh Period**
- **All Inputs, Outputs, Clocks Fully TTL Compatible**
- **3-State Unlatched Output**
- **Common I/O Capability with "Early Write" Feature**
- **Page-Mode Operation for Faster Access**
- **Low Power Dissipation**
  - **Operating . . . 125 mW (typ.)**
  - **Standby . . . 17.5 mW (typ.)**
- **New SMOS (Scaled-MOS) N-Channel Technology**

16-PIN CERAMIC AND PLASTIC DUAL-IN-LINE PACKAGES (TOP VIEW)



18-PIN PLASTIC CHIP CARRIER PACKAGE (TOP VIEW)



PIN NOMENCLATURE	
A0-A7	Address Inputs
CAS	Column Address Strobe
D	Data In
NC	No-Connect
Q	Data Out
RAS	Row Address Strobe
W	Write Enable
V_{DD}	+5 V Supply
V_{SS}	Ground

description

The TMS 4164 is a high-speed, 65,536-bit, dynamic random-access memory, organized as 65,536 words of one bit each. It employs state-of-the-art SMOS (scaled MOS) N-channel double-level polysilicon gate technology for very high performance combined with low cost and improved reliability.

The TMS 4164 features RAS access times of 120 ns, 150 ns, 200 ns, or 250 ns maximum. Power dissipation is 125 mW typical operating, 17.5 mW typical standby.

Refresh period is extended to 4 milliseconds, and during this period each of the 256 rows must be strobed with RAS in order to retain data. CAS can remain high during the refresh sequence to conserve power.

All inputs and outputs, including clocks, are compatible with Series 74 TTL. All address lines and data-in are latched on chip to simplify system design. Data-out is unlatched to allow greater system flexibility. Pin 1 has no internal connection to allow compatibility with other 64K RAMs that use this pin for an additional function.

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The TMS 4164 is offered in a 16-pin dual-in-line ceramic sidebraze package or plastic package and is guaranteed for operation from 0 °C to 70 °C. These packages are designed for insertion in mounting-hole rows on 300 mil (7.62 mm) centers. An 18-pin plastic chip carrier (FP suffix) package is also available.

operation

address (A0 through A7)

Sixteen address bits are required to decode 1 of 65,536 storage cell locations. Eight row-address bits are set up on pins A0 through A7 and latched onto the chip by the row-address strobe ($\overline{RAS}$). Then the eight column-address bits are set up on Pins A0 through A7 and latched onto the chip by the column-address strobe ($\overline{CAS}$). All addresses must be stable on or before the falling edges of $\overline{RAS}$ and $\overline{CAS}$. $\overline{RAS}$ is similar to a chip enable in that it activates the sense amplifiers as well as the row decoder. $\overline{CAS}$ is used as a chip select activating the column decoder and the input and output buffers.

write enable ($\overline{W}$)

The read or write mode is selected through the write enable ($\overline{W}$) input. A logic high on the $\overline{W}$ input selects the read mode and a logic low selects the write mode. The write enable terminal can be driven from standard TTL circuits without a pull-up resistor. The data input is disabled when the read mode is selected. When $\overline{W}$ goes low prior to $\overline{CAS}$, data-out will remain in the high-impedance state for the entire cycle permitting common I/O operation.

data-in (D)

Data is written during a write or read-modify write cycle. Depending on the mode of operation, the falling edge of $\overline{CAS}$ or $\overline{W}$ strobes data into the on-chip data latch. This latch can be driven from standard TTL circuits without a pull-up resistor. In an early-write cycle, $\overline{W}$ is brought low prior to $\overline{CAS}$ and the data is strobed in by $\overline{CAS}$ with setup and hold times referenced to this signal. In a delayed write or read-modify write cycle, $\overline{CAS}$ will already be low, thus the data will be strobed in by $\overline{W}$ with setup and hold times referenced to this signal.

data-out (Q)

The three-state output buffer provides direct TTL compatibility (no pull-up resistor required) with a fan-out of two Series 74 TTL loads. Data-out is the same polarity as data-in. The output is in the high-impedance (floating) state until $\overline{CAS}$ is brought low. In a read cycle the output goes active after the access time interval $t_{a(C)}$ that begins with the negative transition of $\overline{CAS}$ as long as $t_{a(R)}$ is satisfied. The output becomes valid after the access time has elapsed and remains valid while $\overline{CAS}$ is low; $\overline{CAS}$ going high returns it to a high-impedance state. In an early-write cycle, the output is always in the high-impedance state. In a delayed-write or read-modify-write cycle, the output will follow the sequence for the read cycle.

refresh

A refresh operation must be performed at least every four milliseconds to retain data. Since the output buffer is in the high-impedance state unless $\overline{CAS}$ is applied, the $\overline{RAS}$-only refresh sequence avoids any output during refresh. Strobing each of the 256 row addresses (A0 through A7) with $\overline{RAS}$ causes all bits in each row to be refreshed. $\overline{CAS}$ can remain high (inactive) for this refresh sequence to conserve power.

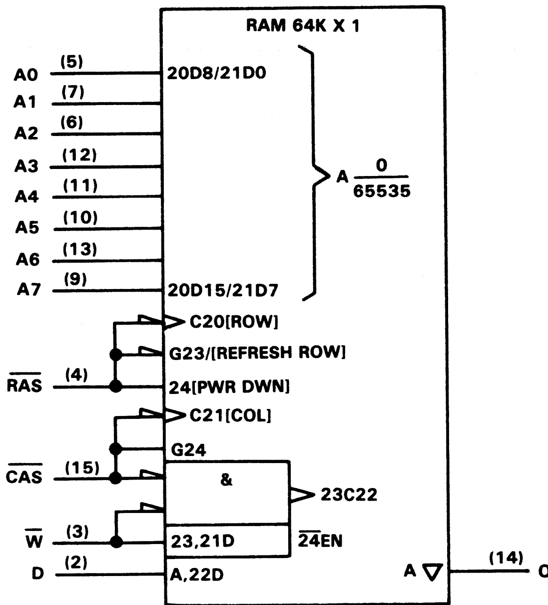
page-mode

Page-mode operation allows effectively faster memory access by keeping the same row address and strobing successive column addresses onto the chip. Thus, the time required to setup and strobe sequential row addresses for the same page is eliminated. To extend beyond the 256 column locations on a single RAM, the row address and $\overline{RAS}$ are applied to multiple 64K RAMs. $\overline{CAS}$ is then decoded to select the proper RAM.

power-up

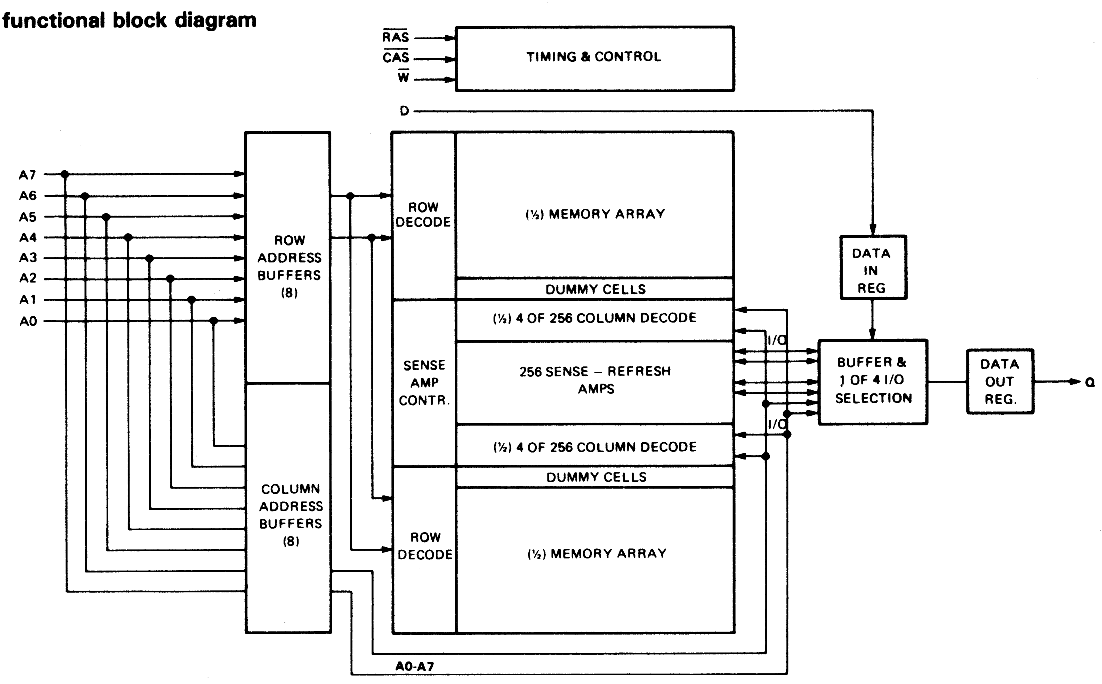
After power-up, the power supply must remain at its steady-state value for 1 ms. In addition, $\overline{RAS}$ must remain high for 100 μs immediately prior to initialization. Initialization consists of performing eight $\overline{RAS}$ cycles before proper device operation is achieved.

logic symbol†



† This symbol is in accordance with IEEE Std 91/ANSI Y32.14 and recent decisions by IEEE and IEC. See explanation on page 289.

functional block diagram



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)*

Voltage on any pin except V_{DD} and data out (see Note 1) . . . . –1.5 to 10 V
Voltage on V_{DD} supply and data out with respect to V_{SS} . . . . –1 to 6 V
Short circuit output current . . . . 50 mA
Power dissipation . . . . 1 W
Operating free-air temperature range . . . . 0°C to 70°C
Storage temperature range . . . . –65°C to 150°C

NOTE 1: All voltage values in this data sheet are with respect to V_{SS}.

* Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the "Recommended Operating Conditions" section of this specification is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

PARAMETER	MIN	NOM	MAX	UNIT
Supply voltage, V_{DD}	4.5	5	5.5	V
Supply voltage, V_{SS}		0		V
High-level input voltage, V_{IH}	2.4		V_{DD}+0.3	V
Low-level input voltage, V_{IL} (see Note 2)	–1		0.8	V
Operating free-air temperature, T_A	0		70	°C

NOTE 2: The algebraic convention, where the more negative (less positive) limit is designated as minimum, is used in this data sheet for logic voltage levels only.

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electrical characteristics over full ranges of recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	TMS 4164-12			TMS 4164-15			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{OH}	High-level output voltage	I_{OH} = −5 mA	2.4			2.4			V
V_{OL}	Low-level output voltage	I_{OL} = 4.2 mA			0.4			0.4	V
I_I	Input current (leakage)	V_I=0 V to 5.8 V, V_{DD}=5 V, All other pins = 0 V			±10			±10	μA
I_O	Output current (leakage)	V_O = 0.4 to 5.5 V, V_{DD} = 5 V, $\overline{CAS}$ high			±10			±10	μA
I_{DD1}*	Average operating current during read or write cycle	t_c = minimum cycle		35	45		28	39	mA
I_{DD2}**	Standby current	After 1 memory cycle, $\overline{RAS}$ and $\overline{CAS}$ high		3.5	5		3.5	5	mA
I_{DD3}*	Average refresh current	t_c = minimum cycle, $\overline{RAS}$ low, $\overline{CAS}$ high		25	35		22	30	mA
I_{DD4}	Average page-mode current	$t_{c(P)}$ = minimum cycle, $\overline{RAS}$ low, $\overline{CAS}$ cycling		25	35		22	30	mA

PARAMETER		TEST CONDITIONS	TMS 4164-20			TMS 4164-25			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{OH}	High-level output voltage	I_{OH} = −5 mA	2.4			2.4			V
V_{OL}	Low-level output voltage	I_{OL} = 4.2 mA			0.4			0.4	V
I_I	Input current (leakage)	V_I=0 V to 5.8 V, V_{DD}=5 V, All other pins = 0 V			±10			±10	μA
I_O	Output current (leakage)	V_O = 0.4 to 5.5 V, V_{DD} = 5 V, $\overline{CAS}$ high			±10			±10	μA
I_{DD1}*	Average operating current during read or write cycle	t_c = minimum cycle		24	34		21	29	mA
I_{DD2}**	Standby current	After 1 memory cycle, $\overline{RAS}$ and $\overline{CAS}$ high		3.5	5		3.5	5	mA
I_{DD3}*	Average refresh current	t_c = minimum cycle, $\overline{RAS}$ low, $\overline{CAS}$ high		19	26		16	22	mA
I_{DD4}	Average page-mode current	$t_{c(P)}$ = minimum cycle, $\overline{RAS}$ low, $\overline{CAS}$ cycling		19	26		16	22	mA

† All typical values are at T_A = 25 °C and nominal supply voltages.
* Additional information on last page.
** V_{IL} > −0.6 V.

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capacitance over recommended supply voltage range and operating free-air temperature range, f = 1 MHz

PARAMETER		TYP†	MAX	UNIT
$C_{i(A)}$	Input capacitance, address inputs	4	7	pF
$C_{i(D)}$	Input capacitance, data input	4	7	pF
$C_{i(RC)}$	Input capacitance strobe inputs	8	10	pF
$C_{i(W)}$	Input capacitance, write enable input	8	10	pF
C_o	Output capacitance	5	8	pF

† All typical values are at T_A = 25 °C and nominal supply voltages.

switching characteristics over recommended supply voltage range and operating free-air temperature range

PARAMTER		TEST CONDITIONS	ALT. SYMBOL	TMS 4164-12		TMS 4164-15		UNIT
				MIN	MAX	MIN	MAX	
$t_{a(C)}$	Access time from $\overline{CAS}$	C_L = 100 pF, Load = 2 Series 74 TTL gates	t_{CAC}		75		100	ns
$t_{a(R)}$	Access time from $\overline{RAS}$	t_{RLCL} = MAX, Load = 2 Series 74 TTL gates	t_{RAC}		120		150	ns
$t_{dis(CH)}$	Output disable time after $\overline{CAS}$ high	C_L = 100 pF, Load = 2 Series 74 TTL gates	t_{OFF}	0	40	0	40	ns

PARAMETER		TEST CONDITIONS	ALT. SYMBOL	TMS 4164-20		TMS 4164-25		UNIT
				MIN	MAX	MIN	MAX	
$t_{a(C)}$	Access time from $\overline{CAS}$	C_L = 100 pF, Load = 2 Series 74 TTL gates	t_{CAC}		135		165	ns
$t_{a(R)}$	Access time from $\overline{RAS}$	t_{RLCL} = MAX, Load = 2 Series 74 TTL gates	t_{RAC}		200		250	ns
$t_{dis(CH)}$	Output disable time after $\overline{CAS}$ high	C_L = 100 pF, Load = 2 Series 74 TTL gates	t_{OFF}	0	50	0	60	ns

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timing requirements over recommended supply voltage range and operating free-air temperature range

PARAMETER		ALT. SYMBOL	TMS 4164-12		TMS 4164-15		UNIT
			MIN	MAX	MIN	MAX	
$t_{c(P)}$	Page mode cycle time	t_{PC}	140		160		ns
$t_{c(rd)}$	Read cycle time*	t_{RC}	230		260		ns
$t_{c(W)}$	Write cycle time	t_{WC}	230		260		ns
$t_{c(rdW)}$	Read-write/read-modify-write cycle time	t_{RWC}	260		285		ns
$t_{w(CH)}$	Pulse width, $\overline{CAS}$ high (precharge time)**	t_{CP}	50		50		ns
$t_{w(CL)}$	Pulse width, $\overline{CAS}$ low†	t_{CAS}	75	10,000	100	10,000	ns
$t_{w(RH)}$	Pulse width, $\overline{RAS}$ high (precharge time)	t_{RP}	100		100		ns
$t_{w(RL)}$	Pulse width, $\overline{RAS}$ low‡	t_{RAS}	120	10,000	150	10,000	ns
$t_{w(W)}$	Write pulse width	t_{WP}	45		45		ns
t_t	Transition times (rise and fall) for $\overline{RAS}$ and $\overline{CAS}$	t_T	3	50	3	50	ns
$t_{su(CA)}$	Column address setup time	t_{ASC}	0		−5		ns
$t_{su(RA)}$	Row address setup time	t_{ASR}	0		0		ns
$t_{su(D)}$	Data setup time	t_{DS}	0		0		ns
$t_{su(rd)}$	Read command setup time	t_{RCS}	0		0		ns
$t_{su(WCH)}$	Write command setup time before $\overline{CAS}$ high	t_{CWL}	50		60		ns
$t_{su(WRH)}$	Write command setup time before $\overline{RAS}$ high	t_{RWL}	50		60		ns
$t_{h(CLCA)}$	Column address hold time after $\overline{CAS}$ low	t_{CAH}	45		45		ns
$t_{h(RA)}$	Row address hold time	t_{RAH}	15		20		ns
$t_{h(RLCA)}$	Column address hold time after $\overline{RAS}$ low	t_{AR}	90		95		ns
$t_{h(CLD)}$	Data hold time after $\overline{CAS}$ low	t_{DH}	50		60		ns
$t_{h(RLD)}$	Data hold time after $\overline{RAS}$ low	t_{DHR}	95		110		ns
$t_{h(WLD)}$	Data hold time after $\overline{W}$ low	t_{DH}	45		45		ns
$t_{h(CHrd)}$	Read command hold time after $\overline{CAS}$ high	t_{RCH}	0		0		ns
$t_{h(RHrd)}$	Read command hold time after $\overline{RAS}$ high	t_{RRH}	5		5		ns
$t_{h(CLW)}$	Write command hold time after $\overline{CAS}$ low	t_{WCH}	50		60		ns
$t_{h(RLW)}$	Write command hold time after $\overline{RAS}$ low	t_{WCR}	95		110		ns
t_{RLCH}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ high	t_{CSH}	120		150		ns
t_{CHRL}	Delay time, $\overline{CAS}$ high to $\overline{RAS}$ low	t_{CRP}	0		0		ns
t_{CLRH}	Delay time, $\overline{CAS}$ low to $\overline{RAS}$ high	t_{RSH}	75		100		ns
t_{CLWL}	Delay time, $\overline{CAS}$ low to $\overline{W}$ low (read-modify-write cycle only)	t_{CWD}	50		60		ns
t_{RLCL}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ low (maximum value specified only to guarantee access time)	t_{RCD}	15	45	20	50	ns
t_{RLWL}	Delay time, $\overline{RAS}$ low to $\overline{W}$ low (read-modify-write cycle only)	t_{RWD}	95		110		ns
t_{WLCL}	Delay time, $\overline{W}$ low to $\overline{CAS}$ low (early write cycle)	t_{WCS}	−5		−5		ns
t_{rf}	Refresh time interval	t_{REF}		4		4	ms

NOTE: Timing measurements are made at the 10% and 90% points of input and clock transitions. In addition, V_{IL} max and V_{IH} min must be met at the 10% and 90% points.

* All cycle times assume t_t = 5 ns.

** Page mode only.

† In a read-modify-write cycle, t_{CLWL} and $t_{su(WCH)}$ must be observed. Depending on the user's transition times, this may require additional $\overline{CAS}$ low time ($t_{w(CL)}$). This applies to page mode read-modify-write also.

‡ In a read-modify-write cycle, t_{RLWL} and $t_{su(WRH)}$ must be observed. Depending on the user's transition times, this may require additional $\overline{RAS}$ low time ($t_{w(RL)}$).

timing requirements over recommended supply voltage range and operating free-air temperature range

PARAMETER		ALT. SYMBOL	TMS 4164-20		TMS 4164-25		UNIT
			MIN	MAX	MIN	MAX	
$t_{c(P)}$	Page mode cycle time	t_{PC}	225		275		ns
$t_{c(rd)}$	Read cycle time*	t_{RC}	330		410		ns
$t_{c(W)}$	Write cycle time	t_{WC}	330		410		ns
$t_{c(rdW)}$	Read-write/read-modify-write cycle time	t_{RWC}	345		455		ns
$t_{w(CH)}$	Pulse width, $\overline{CAS}$ high (precharge time)**	t_{CP}	80		100		ns
$t_{w(CL)}$	Pulse width, $\overline{CAS}$ low†	t_{CAS}	135	10,000	165	10,000	ns
$t_{w(RH)}$	Pulse width, $\overline{RAS}$ high (precharge time)	t_{RP}	120		150		ns
$t_{w(RL)}$	Pulse width, $\overline{RAS}$ low‡	t_{RAS}	200	10,000	250	10,000	ns
$t_{w(W)}$	Write pulse width	t_{WP}	55		75		ns
t_t	Transition times (rise and fall) for $\overline{RAS}$ and $\overline{CAS}$	t_T	3	50	3	50	ns
$t_{su(CA)}$	Column address setup time	t_{ASC}	−5		−5		ns
$t_{su(RA)}$	Row address setup time	t_{ASR}	0		0		ns
$t_{su(D)}$	Data setup time	t_{DS}	0		0		ns
$t_{su(rd)}$	Read command setup time	t_{RCS}	0		0		ns
$t_{su(WCH)}$	Write command setup time before $\overline{CAS}$ high	t_{CWL}	80		100		ns
$t_{su(WRH)}$	Write command setup time before $\overline{RAS}$ high	t_{RWL}	80		100		ns
$t_{h(CLCA)}$	Column address hold time after $\overline{CAS}$ low	t_{CAH}	55		75		ns
$t_{h(RA)}$	Row address hold time	t_{RAH}	25		35		ns
$t_{h(RLCA)}$	Column address hold time after $\overline{RAS}$ low	t_{AR}	140		190		ns
$t_{h(CLD)}$	Data hold time after $\overline{CAS}$ low	t_{DH}	80		110		ns
$t_{h(RLD)}$	Data hold time after $\overline{RAS}$ low	t_{DHR}	145		195		ns
$t_{h(WLD)}$	Data hold time after $\overline{W}$ low	t_{DH}	55		75		ns
$t_{h(CHrd)}$	Read command hold time after $\overline{CAS}$ high	t_{RCH}	0		0		ns
$t_{h(RHrd)}$	Read command hold time after $\overline{RAS}$ high	t_{RRH}	5		5		ns
$t_{h(CLW)}$	Write command hold time after $\overline{CAS}$ low	t_{WCH}	80		110		ns
$t_{h(RLW)}$	Write command hold time after $\overline{RAS}$ low	t_{WCR}	145		195		ns
t_{RLCH}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ high	t_{CSH}	200		250		ns
t_{CHRL}	Delay time, $\overline{CAS}$ high to $\overline{RAS}$ low	t_{CRP}	0		0		ns
t_{CLRH}	Delay time, $\overline{CAS}$ low to $\overline{RAS}$ high	t_{RSH}	135		165		ns
t_{CLWL}	Delay time, $\overline{CAS}$ low to $\overline{W}$ low (read–modify-write cycle only)	t_{CWD}	65		105		ns
t_{RLCL}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ low (maximum value specified only to guarantee access time)	t_{RCD}	25	65	35	85	ns
t_{RLWL}	Delay time, $\overline{RAS}$ low to $\overline{W}$ low (read–modify-write cycle only)	t_{RWD}	130		190		ns
t_{WLCL}	Delay time, $\overline{W}$ low to $\overline{CAS}$ low (early write cycle)	t_{WCS}	−5		−5		ns
t_{rf}	Refresh time interval	t_{REF}		4		4	ms

NOTE: Timing measurements are made at the 10% and 90% points of input and clock transitions. In addition, V_{IL} max and V_{IH} min must be met at the 10% and 90% points.

* All cycle times assume t_t = 5 ns.

** Page mode only.

† In a read-modify-write cycle, t_{CLWL} and $t_{su(WCH)}$ must be observed. Depending on the user's transition times, this may require additional $\overline{CAS}$ low time ($t_{w(CL)}$). This applies to page mode read-modify-write also.

‡ In a read-modify-write cycle, t_{RLWL} and $t_{su(WRH)}$ must be observed. Depending on the user's transition times, this may require additional $\overline{RAS}$ low time ($t_{w(RL)}$).

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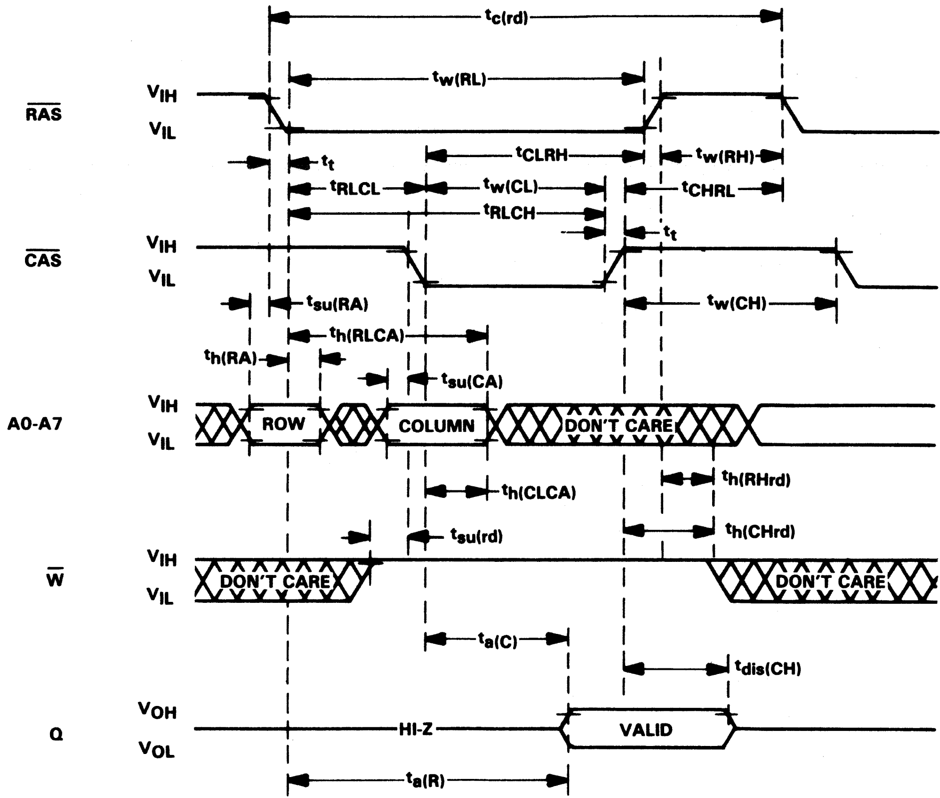
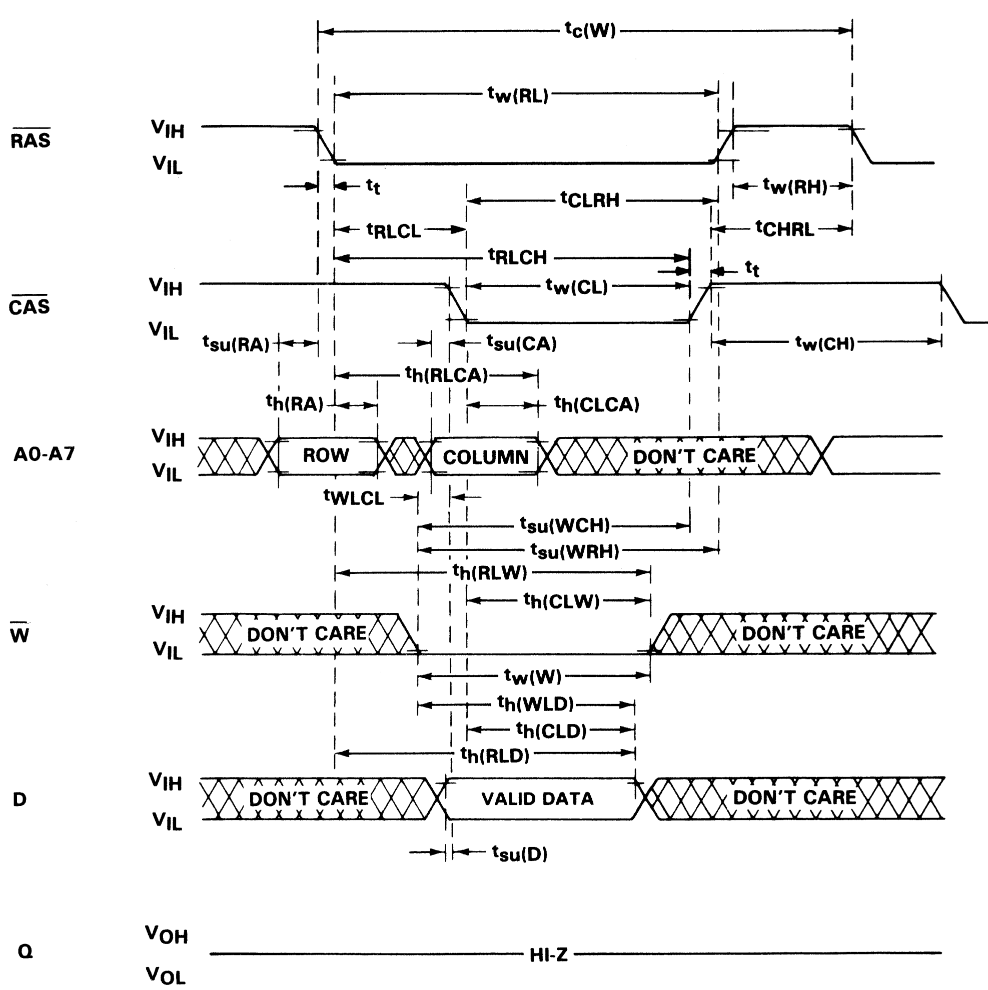
read cycle timing



early write cycle timing



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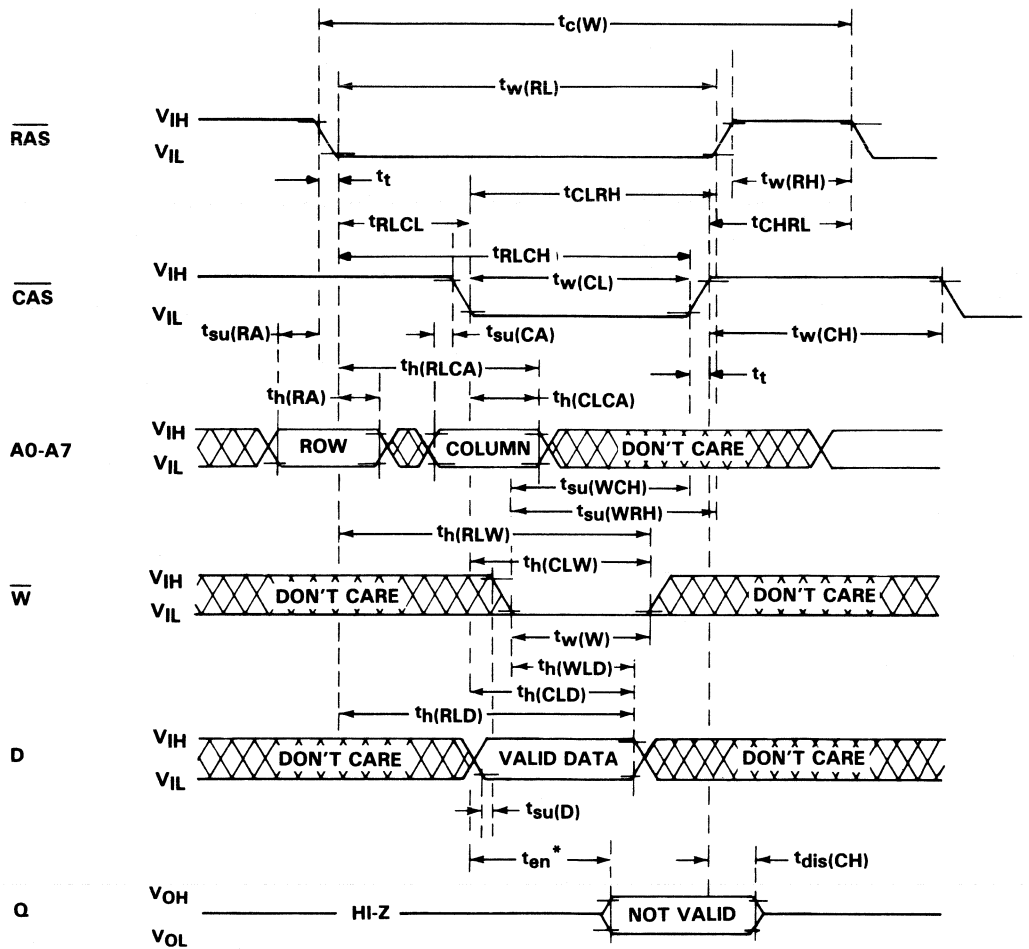
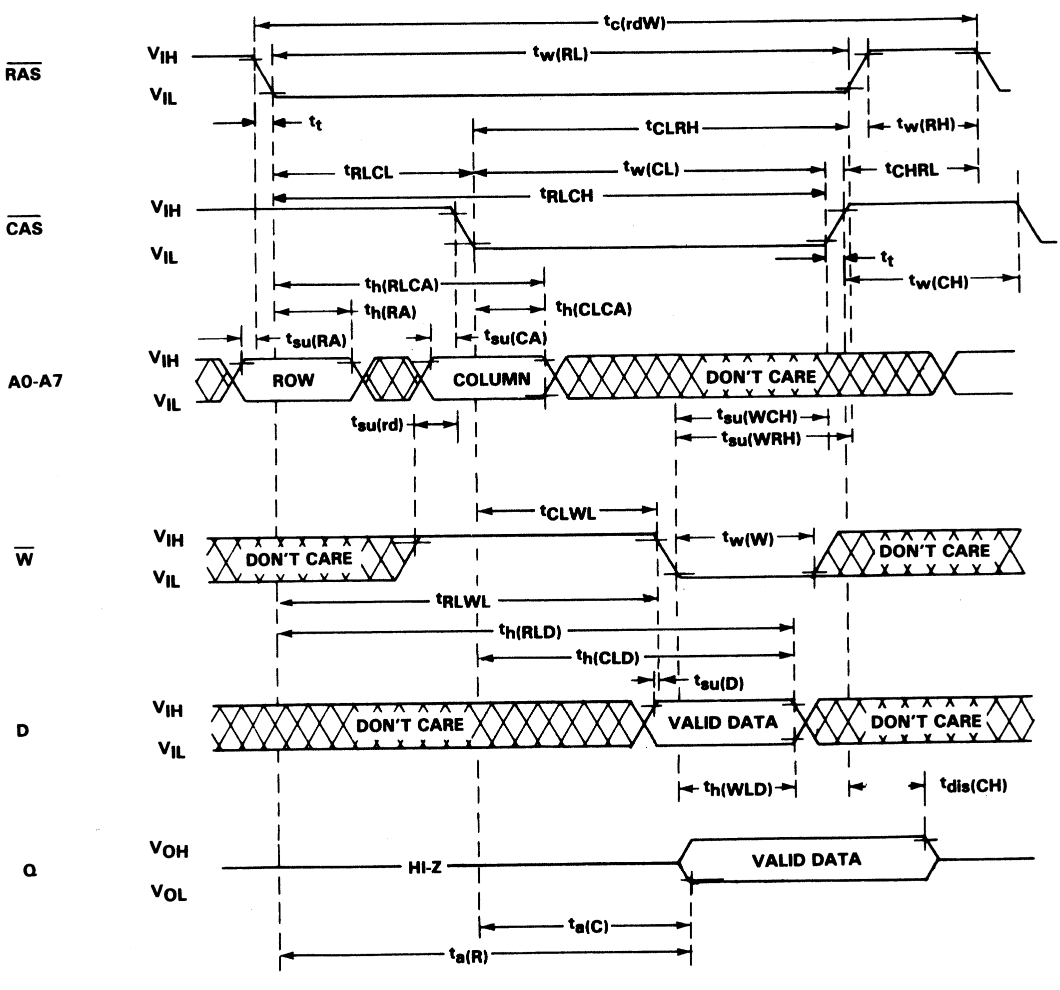
write cycle timing



* The enable time (t_{en}) for a write cycle is equal in duration to the access time from $\overline{CAS}$ ($t_{a(C)}$) in a read cycle; but the active levels at the output are invalid.

read-write/read-modify-write cycle timing



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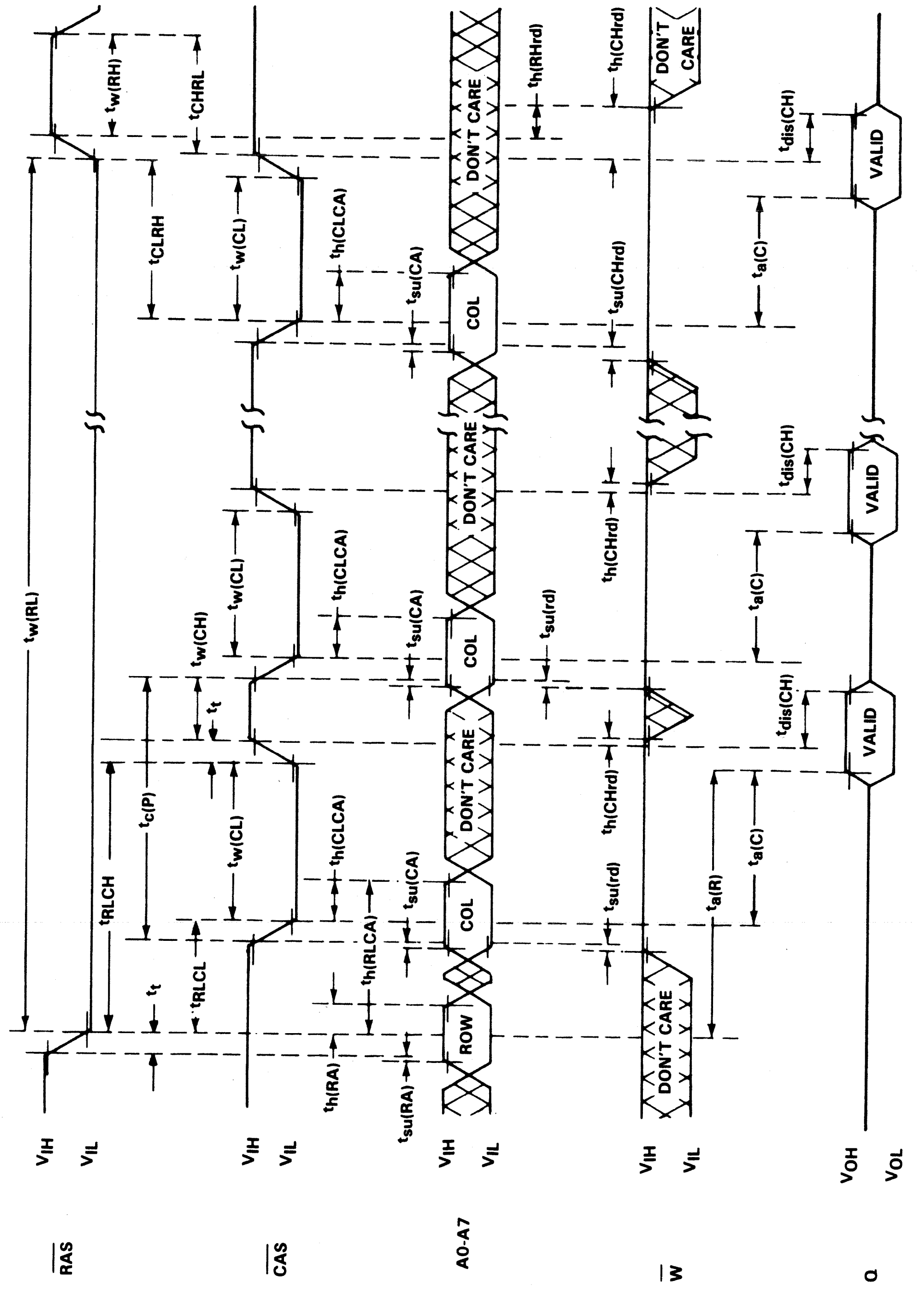
page-mode read cycle timing



NOTE: A write cycle or a read-modify-write cycle can be intermixed with read cycles as long as the write and read-modify-write timing specifications are not violated.

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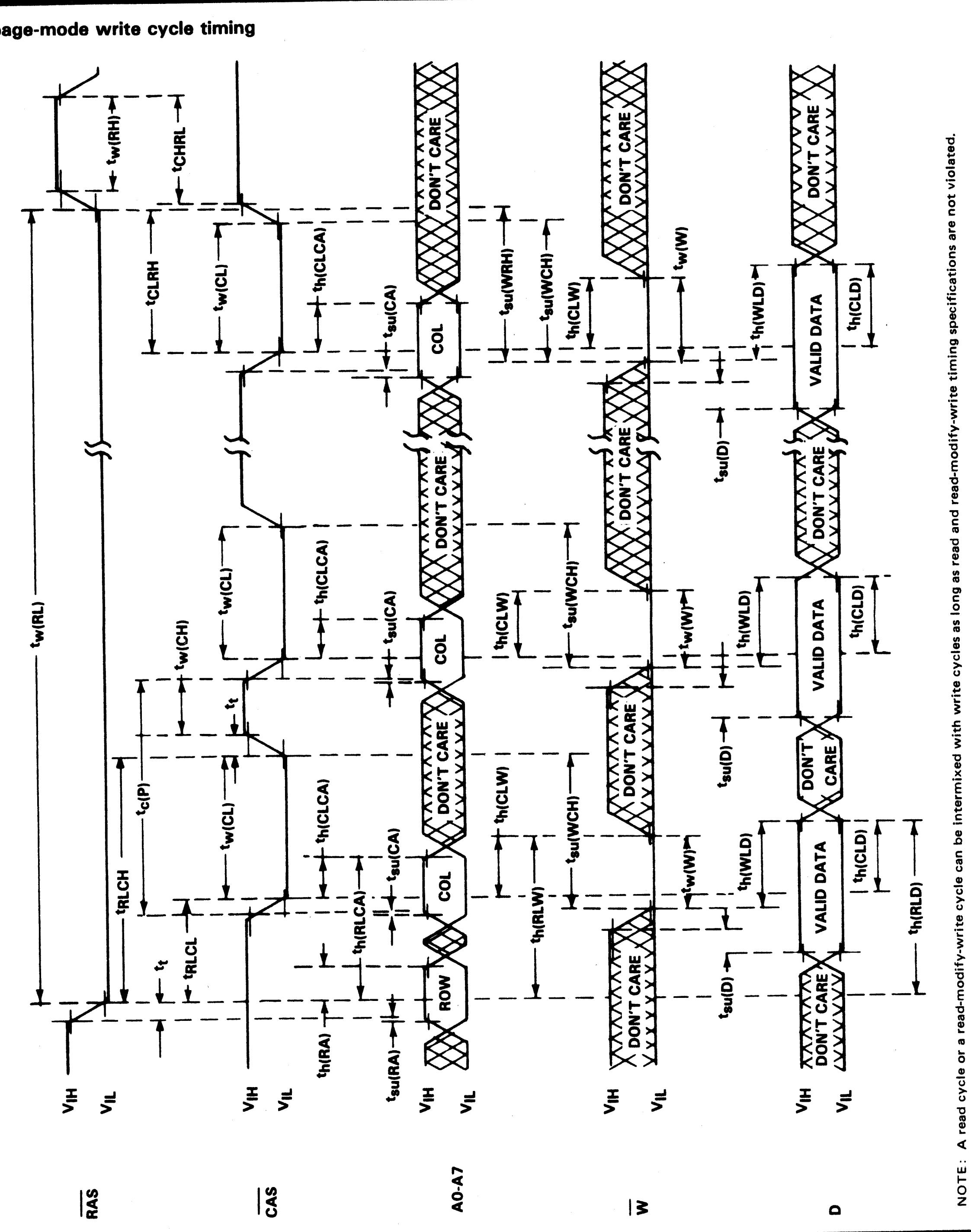
page-mode write cycle timing



NOTE: A read cycle or a read-modify-write cycle can be intermixed with write cycles as long as read and read-modify-write timing specifications are not violated.

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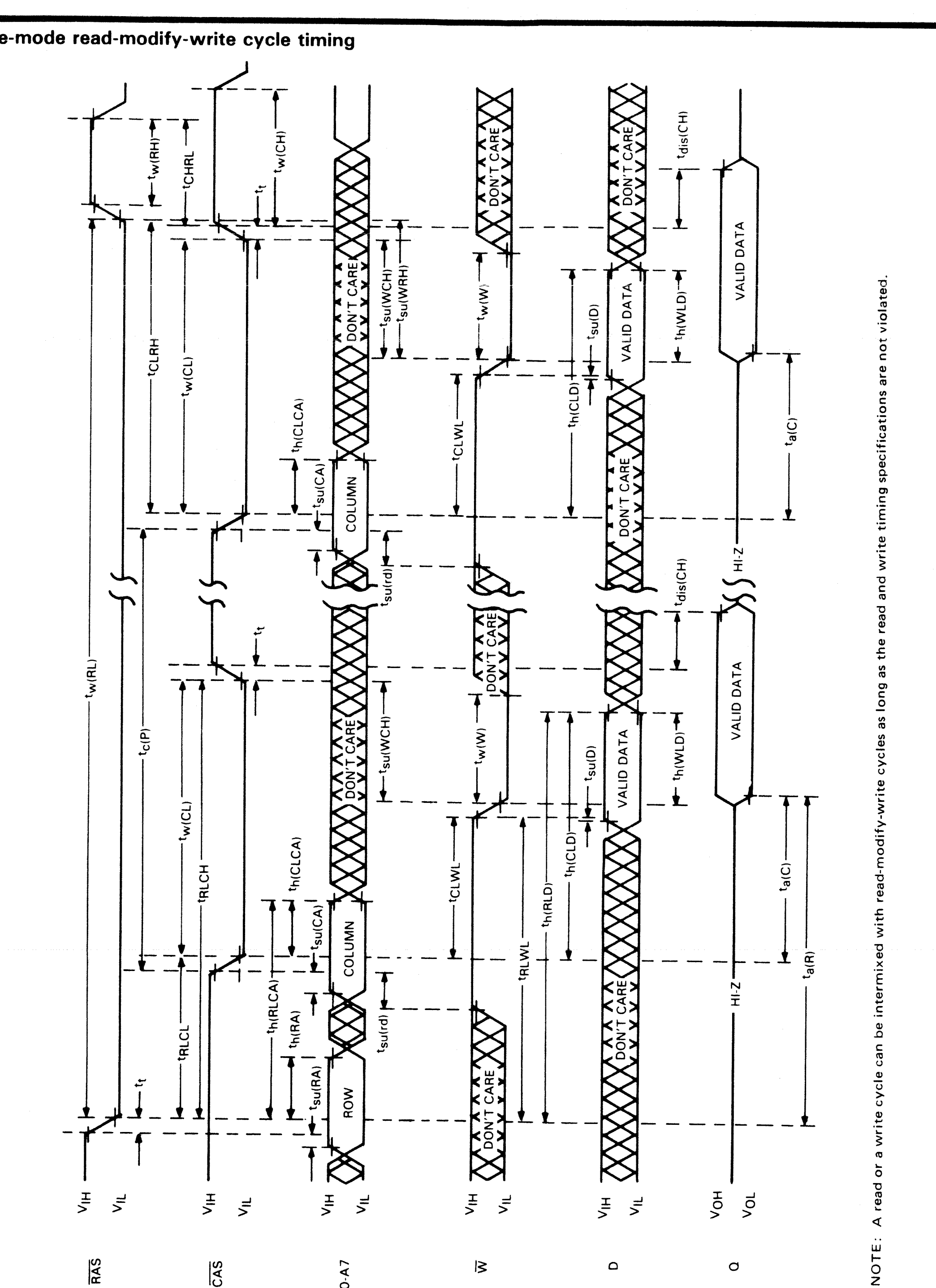
page-mode read-modify-write cycle timing



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$\overline{RAS}$-only refresh timing

$t_{c(rd)}$
$t_{w(RL)}$
$t_{w(RH)}$
t_t
t_t
$t_{h(RA)}$
$t_{su(RA)}$

$\overline{RAS}$ V_{IH} V_{IL}

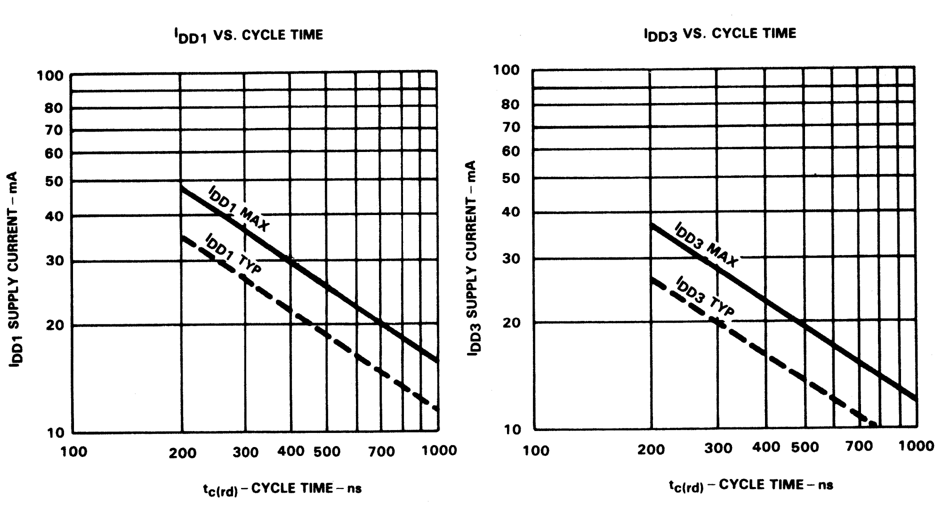
$\overline{CAS}$ V_{IH} V_{IL} DON'T CARE DON'T CARE

A0-A7 V_{IH} V_{IL} DON'T CARE ROW DON'T CARE

$\overline{W}$ V_{IH} V_{IL} DON'T CARE

D V_{IH} V_{IL} DON'T CARE

Q V_{OH} V_{OL} HI-Z



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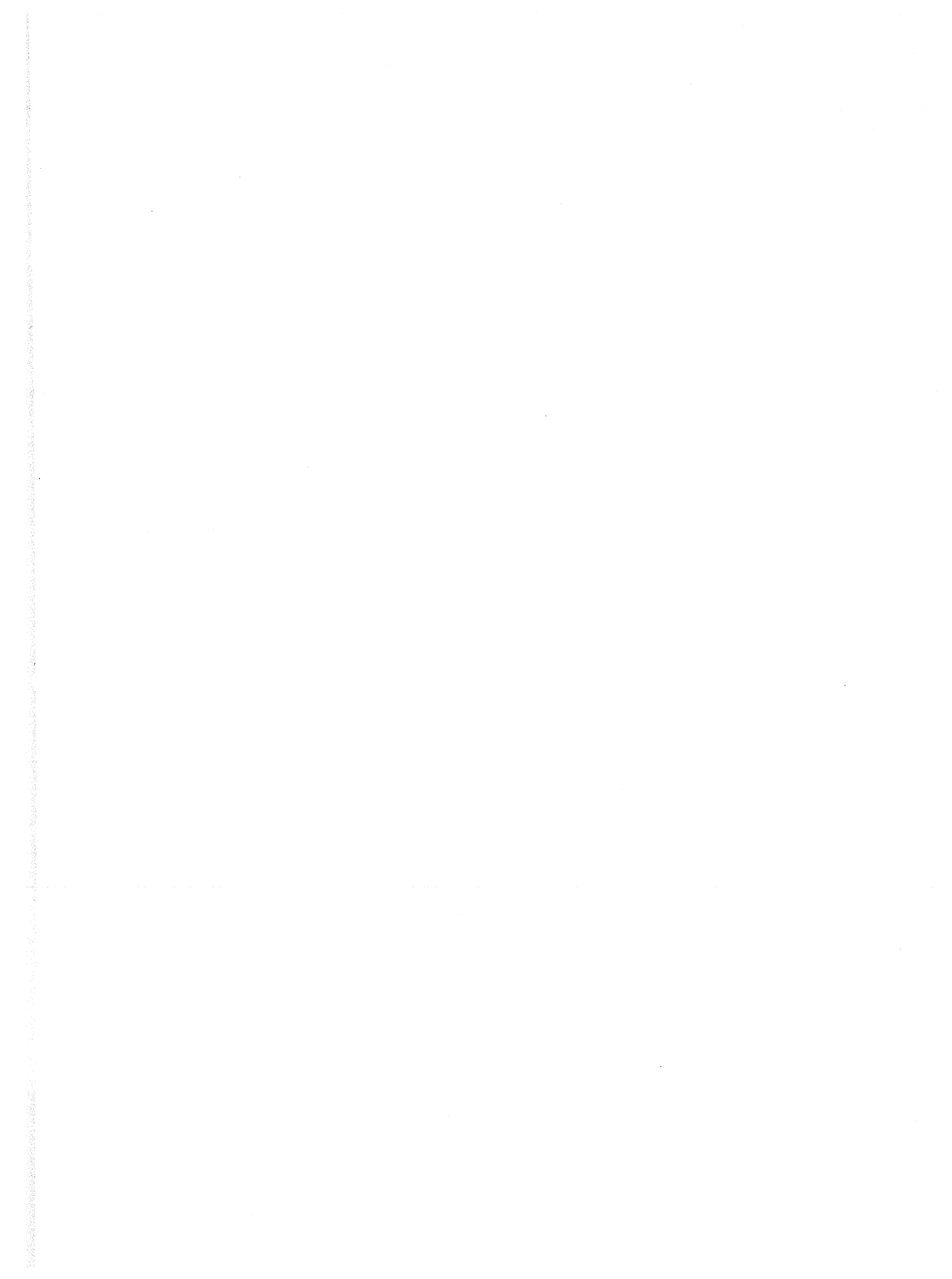

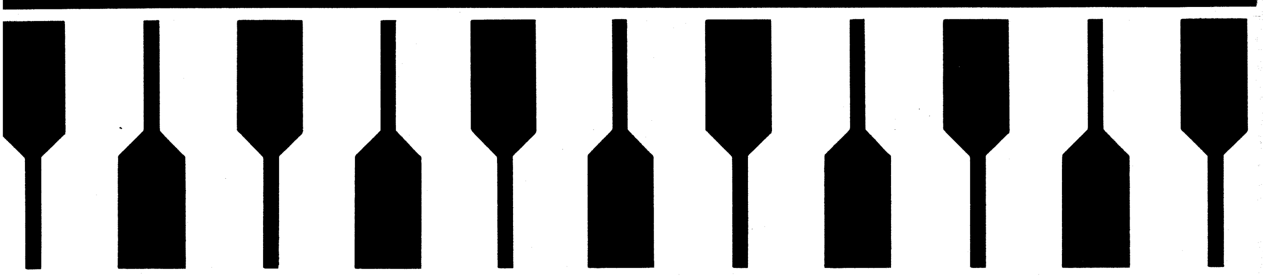

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